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Road vehicles — Media Oriented Systems Transport (MOST) —

Part 11: 150-Mbit/s coaxial physical layer conformance test plan

Véhicules routiers — Système de transport axé sur les médias —

Partie 11: Plan d'essais de conformité de la couche coaxiale physique à 150 Mbit/s

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Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

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For an explanation of the voluntary nature of standards, the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT), see www.iso.org/iso/foreword.html.

This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

A list of all parts in the ISO 21806 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Introduction

The Media Oriented Systems Transport (MOST) communication technology was initially developed at the end of the 1990s in order to support complex audio applications in cars. The MOST Cooperation was founded in 1998 with the goal to develop and enable the technology for the automotive industry. Today, MOST[1)] enables the transport of high Quality of Service (QoS) audio and video together with packet data and real-time control to support modern automotive multimedia and similar applications. MOST is a function-oriented communication technology to network a variety of multimedia devices comprising one or more MOST nodes.

Figure 1 shows a MOST network example.

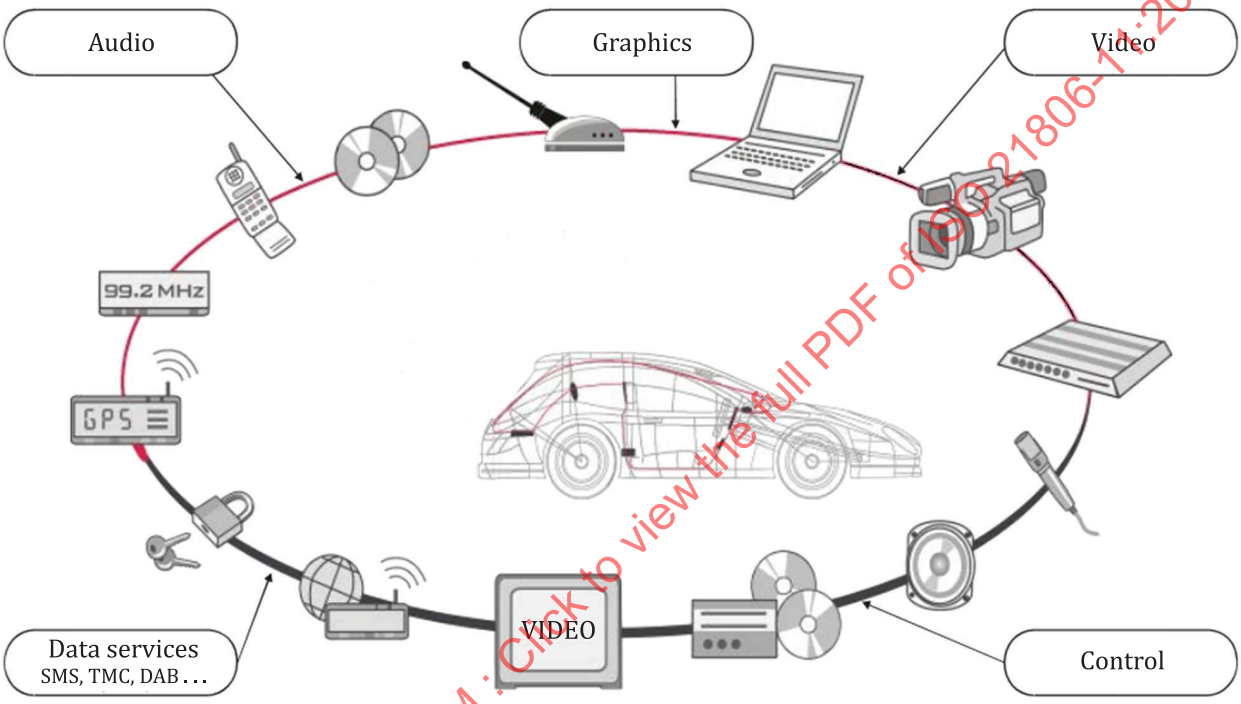

Figure 1 — MOST network example

The MOST communication technology provides:

— synchronous and isochronous streaming,

— small overhead for administrative communication control,

— a functional and hierarchical system model,

— API standardization through a function block (FBlock) framework,

— free partitioning of functionality to real devices,

— service discovery and notification, and

— flexibly scalable automotive-ready Ethernet communication according to ISO/IEC/IEEE 8802-3[2].

MOST is a synchronous time-division-multiplexing (TDM) network that transports different data types on separate channels at low latency. MOST supports different bit rates and physical layers. The network clock is provided with a continuous data signal.

1) MOST® is the registered trademark of Microchip Technology Inc. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO.

Within the synchronous base data signal, the content of multiple streaming connections and control data is transported. For streaming data connections, bandwidth is reserved to avoid interruptions, collisions, or delays in the transport of the data stream.

MOST specifies mechanisms for sending an isochronous, packet-based data in addition to control data and streaming data. The transmission of packet-based data is separated from the transmission of control data and streaming data. None of them interfere with each other.

A MOST network consists of devices that are connected to one common control channel and packet channel.

In summary, MOST is a network that has mechanisms to transport the various signals and data streams that occur in multimedia and infotainment systems.

The ISO Standards Maintenance Portal (https://standards.iso.org/iso/) provides references to MOST specifications implemented in today's road vehicles because easy access via hyperlinks to these specifications is necessary. It references documents that are normative or informative for the MOST versions 4V0, 3V1, 3V0, and 2V5.

The ISO 21806 series has been established in order to specify requirements and recommendations for implementing the MOST communication technology into multimedia devices and to provide conformance test plans for implementing related test tools and test procedures.

To achieve this, the ISO 21806 series is based on the open systems interconnection (OSI) basic reference model in accordance with ISO/IEC 7498-1[1] and ISO/IEC 10731[3], which structures communication systems into seven layers as shown in Figure 2. Stream transmission applications use a direct stream data interface (transparent) to the data link layer.

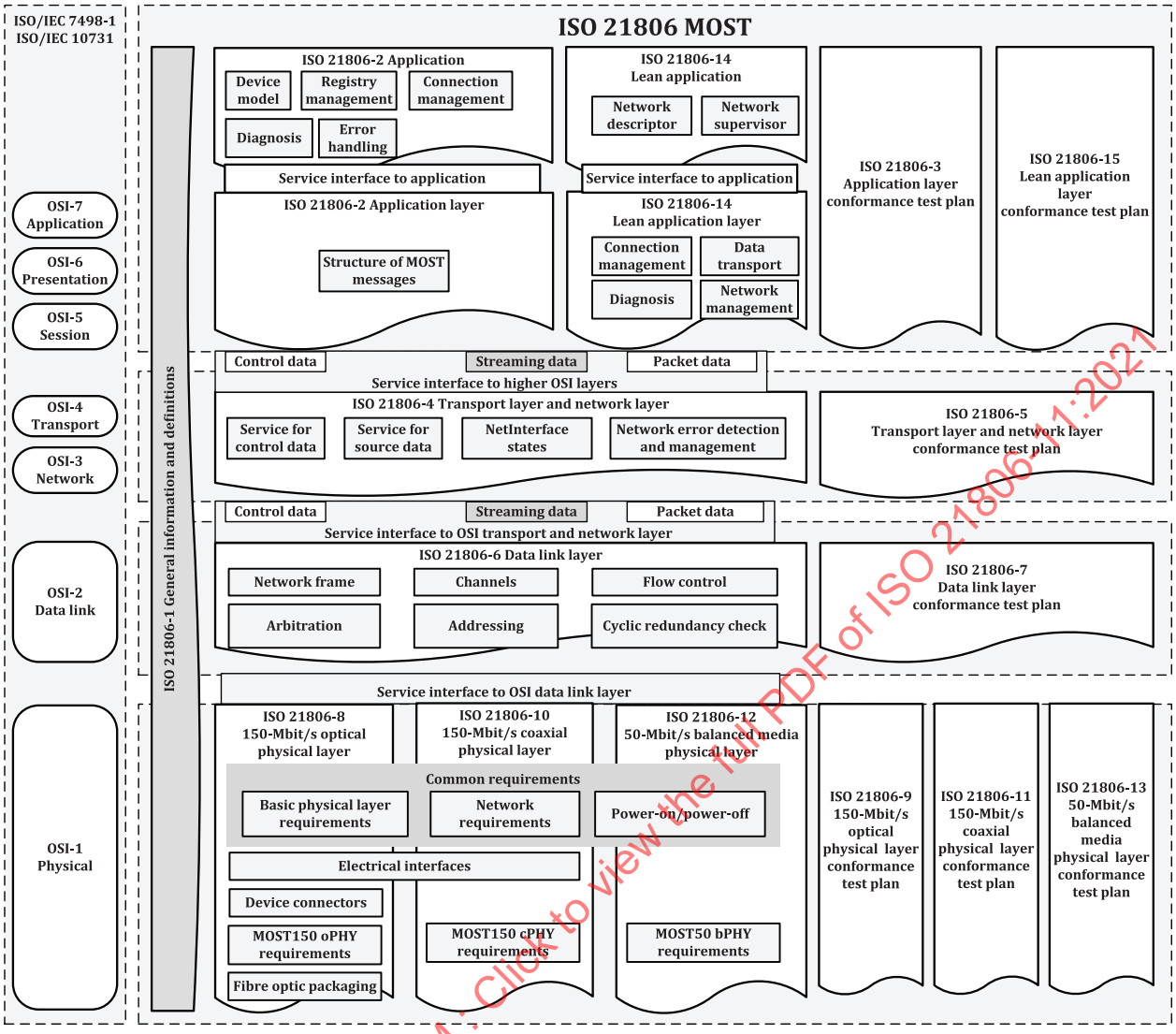

Figure 2 — The ISO 21806 series reference according to the OSI model

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Road vehicles — Media Oriented Systems Transport (MOST) —

Part 11:
150-Mbit/s coaxial physical layer conformance test plan

1 Scope

This document specifies the conformance test plan for the 150-Mbit/s coaxial physical layer for MOST (MOST150 cPHY), a synchronous time-division-multiplexing network.

This document specifies the basic conformance test measurement methods, relevant for verifying compatibility of networks, nodes, and MOST components with the requirements specified in ISO 21806-10.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 21806-1, *Road vehicles — Media Oriented Systems Transport (MOST) — Part 1: General information and definitions*

ISO 21806-10, *Road vehicles — Media Oriented Systems Transport (MOST) — Part 10: 150-Mbit/s coaxial physical layer*

ISO 20860-2, *Road vehicles — 50 ohms impedance radio frequency connection system interface — Part 2: Test procedures*

EN 50289-1-8, *Communication cables — Specifications for test methods — Part 1-8: Electrical test methods — Attenuation*

EN 50289-1-11, *Communication cables — Specifications for test methods — Part 1-11: Electrical test methods — Characteristic impedance, input impedance, return loss*

No JEDEC JESD8C.01,[2] *interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits*

TIA/EIA-644-A-2001,[3] *Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) interface Circuits*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 21806-1, ISO 21806-10 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

2) Available at https://www.jedec.org/.

3) Available at https://www.tiaonline.org/standards/.

— IEC Electropedia: available at http://www.electropedia.org/

3.1
intersymbol interference
disturbance due to the overflowing into the signal element representing a wanted digit of signal elements representing preceding or following digits

[SOURCE: IEC Electropedia 702-08-33]

4 Symbols and abbreviated terms

4.1 Symbols

---	empty table cell or feature undefined
A_{DC_loss}	DC attenuation
F	frequency
ρ_{Fs}	network frame rate
ρ_{BR}	bit rate
v_{RMS}	transferred jitter, calculated using the root-mean-square method
L_{RL}	return loss
V_{RXP}	voltage at the LVDS receive terminal P
V_{RXN}	voltage at the LVDS receive terminal N
V_{TXP}	voltage at the LVDS transmit terminal P
V_{TXN}	voltage at the LVDS transmit terminal N
t	time
T	temperature
T_A	ambient temperature
T_{Typ}	typical temperature
t_{SLS}	start of measurement time
t_{SLE}	end of measurement time

4.2 Abbreviated terms

AC	alternate current
AFE	analogue frontend
AJ	alignment jitter
BR	bit rate
BW	bandwidth

CEC	coaxial electrical converter
CEport	coaxial electrical port (combination of AFE and CEC)
Cfg	configuration
CTR	coaxial transceiver
DC	direct current
DSO	digital sampling oscilloscope
EMD	equilibrium mode power distribution
ECC	electrical coaxial converter
ECport	electrical coaxial port (combination of AFE and ECC)
IUT	implementation under test
MNC	MOST network controller
MTCM	MOST150 cPHY tester cable model
Mux	multiplexer
PCB	printed circuit board
PG	pattern generator
PHYSTT	physical layer stress test tool
PLL	phase lock loop
RMS	root mean square
SDA	serial data analyser
SLE	signal level end
SLS	signal level start
SMD	surface mount device
SP	specification point
TDR	time-domain reflectometer
TJ	transferred jitter
UI	unit interval
VCM	common mode voltage
VNA	vector network analyser

5 Conventions

This document is based on OSI service conventions as specified in ISO/IEC 10731[3].

6 Operating conditions and measurement tools, requested accuracy

6.1 Operating conditions

Temperature range for MOST components: T_A = -40 °C to +105 °C according to ISO 21806-10:2021, 11.3.

Voltage range for MOST components: V_{CCCN} and V_{CCSW}, with an operating range of 3,3 V ± 0,165 V according to ISO 21806-10:2021, Clause 10.

NOTE There are functional requirements for the ECC within an extended voltage supply range according to ISO 21806-10.

6.2 Apparatus — Measurement tools, requested accuracy

Apart from the measurement tools listed in this subclause, depending on the chosen test method and method to generate stimuli for the test, further equipment is necessary (e.g. electrical attenuator, discrete filter module to emulate cable transfer function, etc.). Performance requirements of such equipment depend on the use case.

The following list provides the measurement tools.

6.2.1 Oscilloscope

— digital sampling oscilloscope;

— sampling rate ≥ 10 gigasample/s;

— bandwidth ≥ 1,5 GHz;

— sampling memory ≥ 10 megasample;

— active probe (single-ended, differential).

6.2.2 VNA or TDR (TDR bandwidth ≥ 3,5 GHz).

6.2.3 Ampere meter

— accuracy ≤ 2 µA;

— trigger input (for timing measurements).

6.2.4 Pattern generator for generating MOST150 cPHY stress pattern[7]

— bandwidth 300 Mbit/s;

— trigger output (for timing measurements).

6.2.5 Directional coupler (for duplex set-ups only), the required performance levels are discussed in 10.4.2.

7 Electrical characteristics

7.1 Test according to LVDS

Testing of MOST devices or MOST components shall be performed according to the measurement methods and set-ups specified in TIA/EIA-644-A-2001. Parameters and their respective limits are also derived from TIA/EIA-644-A-2001, with the exception of common mode voltage (V_{CM}) as specified in ISO 21806-10:2021, 12.1.

7.2 Test according to LVTTL

Testing of MOST devices or MOST components shall be performed in accordance with JEDEC No. JESD8C.01.

8 Coaxial characteristics

8.1 High/low detection at SP2

To determine high/low levels, the MOST150 cPHY stress pattern[7] shall be used. At least 500 pulses (5 UI or 6 UI) shall be extracted out of the measured data. Extraction can be done by triggering on pulse width ranges or by software-based selection on a prior acquired waveform. The statistical mean of all amplitude samples lying in the slice between the start of measurement (t_{SLS}) and the end of measurement (t_{SLE}) for all acquired high pulses is defined as high. The statistical mean of all amplitude samples lying in the slice between t_{SLS} and t_{SLE} for all acquired low pulses is defined as low. t_{SLS} and t_{SLE} are defined in this document and shown in Table 1.

Table 1 — Signal level measurement interval

Measurement region	Value	Unit
t_{SLS}	1,00	UI
t_{SLE}	3,00	UI

The measured amplitudes (high and low) are an integral part of further measurements at SP2.

Figure 3 defines the high/low detection at SP2.

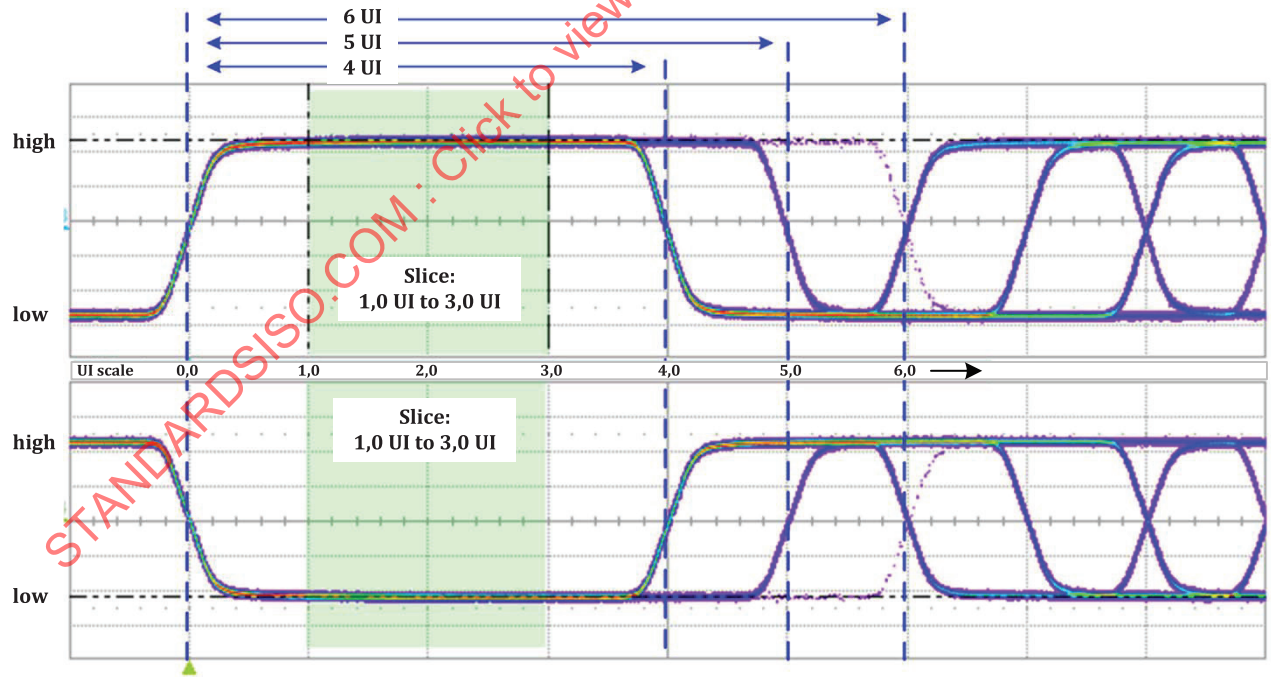


Figure 3 — High/low detection at SP2

8.2 Transition times at SP2

The transition times (rise and fall) are detected as the time of an edge when transitioning through the level range of 20 % and 80 % of the amplitude (high and low, see 8.1). Therefore, high/low detection shall be performed before transition times are determined.

To ensure non-ambiguous measurements the method described below is recommended and applied as a reference procedure in the case of discrepancies.

Formula (1) and Formula (2) define the amplitude threshold levels.

$$h_{20} = \left[(b_1 - b_0) \times 0{,}2 \right] + b_0 \tag{1}$$

$$h_{80} = \left[(b_1 - b_0) \times 0{,}8 \right] + b_0 \tag{2}$$

where

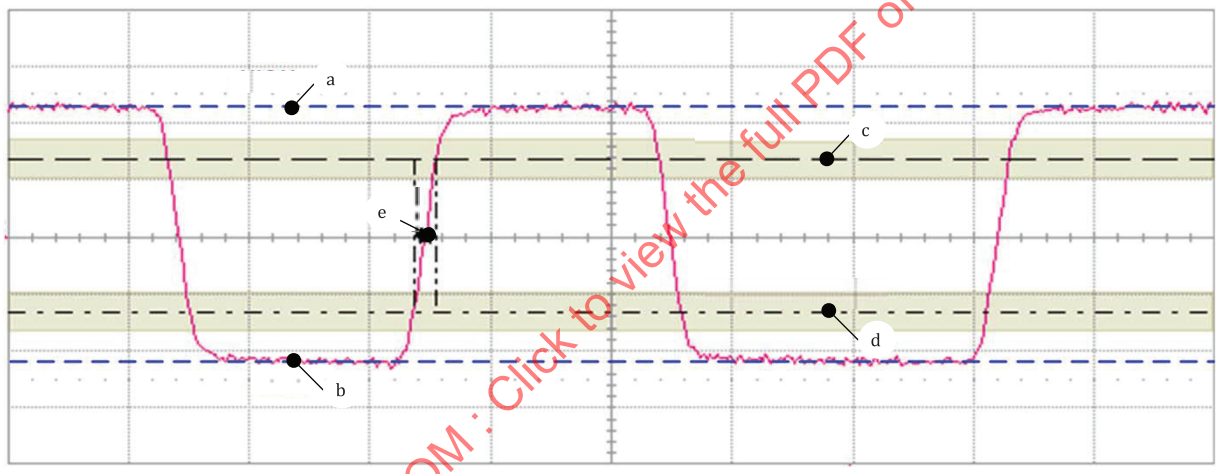
h_{20} is the 20 % threshold of the amplitude;

h_{80} is the 80 % threshold of the amplitude;

b_0 is the signal level when a logic 0 is being transmitted (low);

b_1 is the signal level when a logic 1 is being transmitted (high).

Figure 4 shows an example for the detection of rise-time.



a High.
b Low.
c 80 % threshold.
d 20 % threshold.
e Rise at trigger level.

Figure 4 — Example for detection of rise-time

Measured transition times are smaller than the specified limit in ISO 21806-10:2021, 9.4. MOST150 cPHY stress pattern[7] should be used as data signal.

8.3 Steady state amplitude at SP2

Following the method in 8.1, the steady state amplitude is the difference between high and low.

8.4 Attenuation of coaxial interconnect

8.4.1 General

ISO 21806-10 specifies the attenuation requirements for a coaxial interconnect, formed of one or more cables and the associated couplers and harness connectors. The maximum total length of the interconnect is 15 m. The attenuation of such an interconnect is frequency dependent. ISO 21806-10 specifies an idealized, frequency dependent attenuation function with the coefficients A_{DC_loss} and F_{skin} in Formula (3)

$$A(F) = -A_{DC\_loss} - \sqrt{\frac{F}{F_{skin}}} \tag{3}$$

where

A is the attenuation;

A_{DC_loss} represents the DC attenuation;

F is the frequency;

F_{skin} represents the skin effect losses.

Attenuation requirements are limited to the frequency range between 1 MHz and 450 MHz and the absolute attenuation is allowed to vary, as long as specific requirements are met (see 8.4.5).

8.4.2 Coefficient values based on attenuation measurements

It is determined that the coefficient values calculated (as described below) based on attenuation measurements for the IUT are within the specified limits:

— $A_{DC\_loss} < 0{,}5$ dB;

— $F_{skin} > 9{,}2 \times 10^6$ Hz/dB^2.

8.4.3 Fitting of corridor

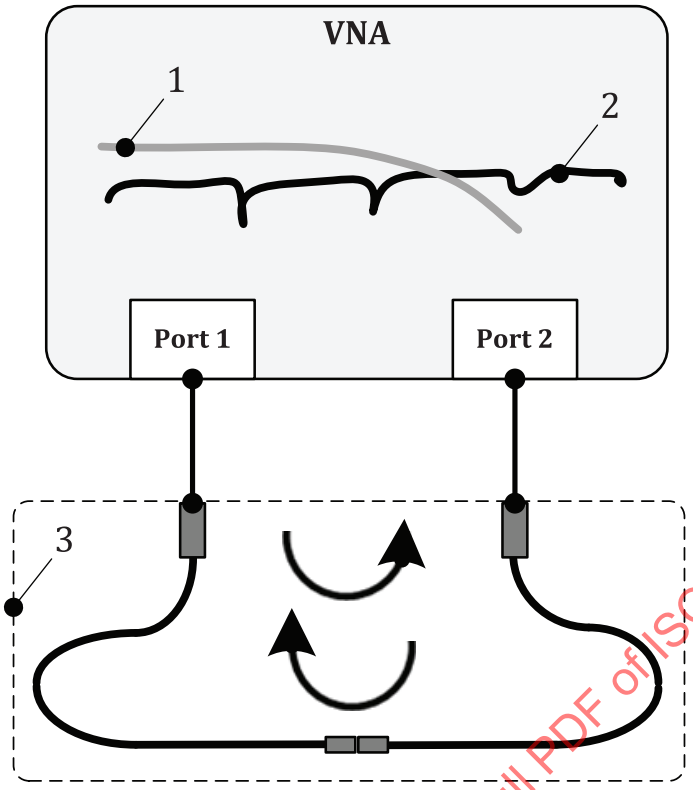
With the evaluated coefficients and the given attenuation function, an idealized attenuation curve can be constructed, which approximates the characteristics of the measured interconnect. ISO 21806-10:2021, 9.4.1 mandates that the difference between data-points of the constructed and the measured attenuation curve (residues) is smaller than ±1 dB.

Attenuation requirements described above apply to the complete temperature range, automotive environmental conditions, and lifetime.

NOTE Although attenuation always reduces signal strength, attenuation in MOST150 cPHY is specified with positive values (e.g. $A_{DC\_loss} < 0{,}5$ dB).

8.4.4 Attenuation test set-up

Figure 5 specifies the attenuation test set-up.



Key

1 attenuation
2 return loss
3 coaxial interconnect

Figure 5 — Attenuation test set-up

8.4.5 Test procedure

8.4.5.1 General

The test procedure shall start with the measurement of the attenuation characteristic over frequency for an IUT.

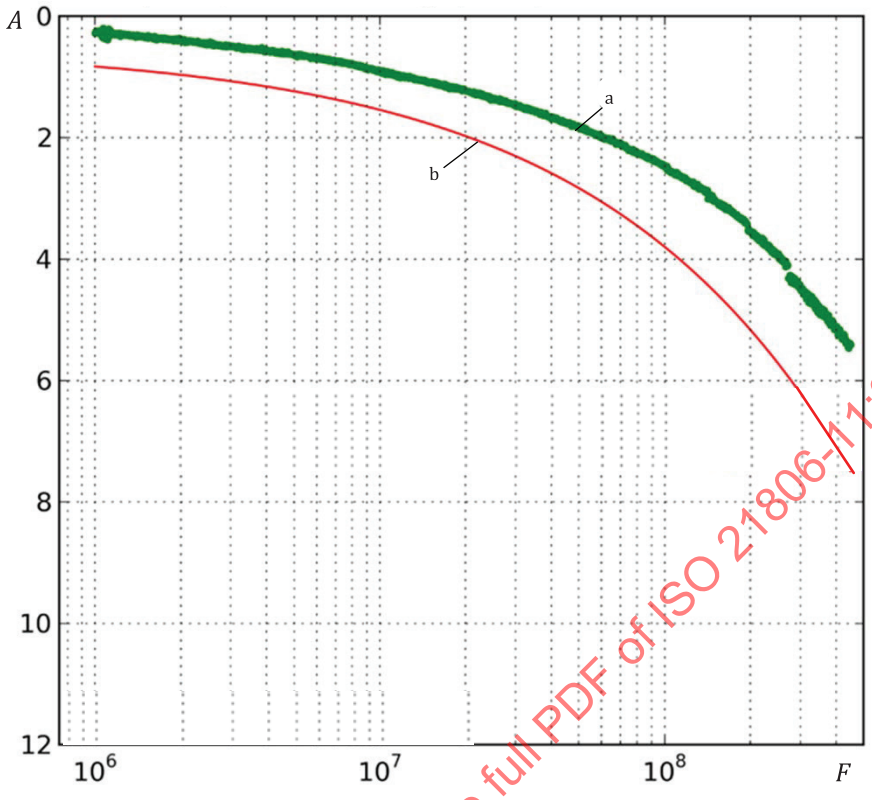
This is usually done with a VNA, using a 2-port arrangement. The VNA measures attenuation from port 1 to port 2 and vice versa.

The frequency sweep shall produce at least 40 data points per decade, logarithmically distributed.

The measurement procedure shall be performed according to EN 50289-1-8.

8.4.5.2 Data acquisition

Figure 6 shows the data acquisition for an IUT cable length of 15 m. See 8.4.2 for A_{DC_loss} and F_{skin} specification limits.



Key

A attenuation [dB]

F frequency [Hz]

a Acquired data in frequency range 1 MHz to 450 MHz.

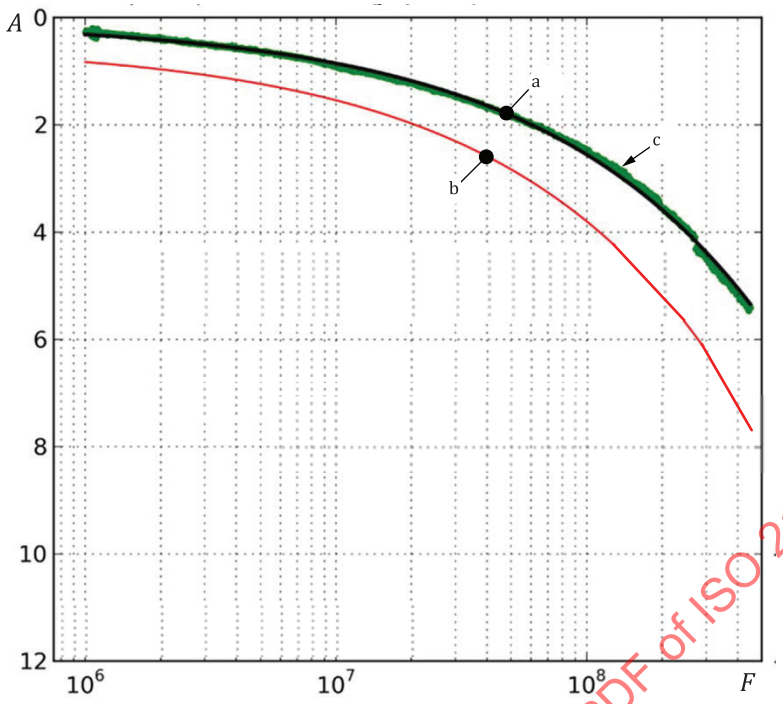
b MOST150 cPHY specification limits, idealized attenuation characteristic based on worst case coefficients A_{DC_loss} and F_{skin}.

Figure 6 — Data acquisition

8.4.5.3 Data fitting

A least square fitting algorithm fits the measured data to the given attenuation function, resulting in values for A_{DC_loss} and F_{skin}. The evaluated coefficients A_{DC_loss} < 0,07 dB and F_{skin} > 1,62 × 10^7 Hz/dB^2 are within the specified limits according to 8.4.2.

Figure 7 shows the data fitting for an IUT cable length of 15 m.



Key

A	attenuation [dB]
F	frequency [Hz]
a	Idealized attenuation curve approximating the measured performance of the IUT (attenuation function, with coefficients as determined by the fit).
b	MOST150 cPHY specification limits: idealized attenuation characteristic based on worst case coefficients A_{DC_loss} and F_{skin}.
c	Acquired data in frequency range 1 MHz to 450 MHz.

Figure 7 — Data fitting

8.4.5.4 Attenuation conformance

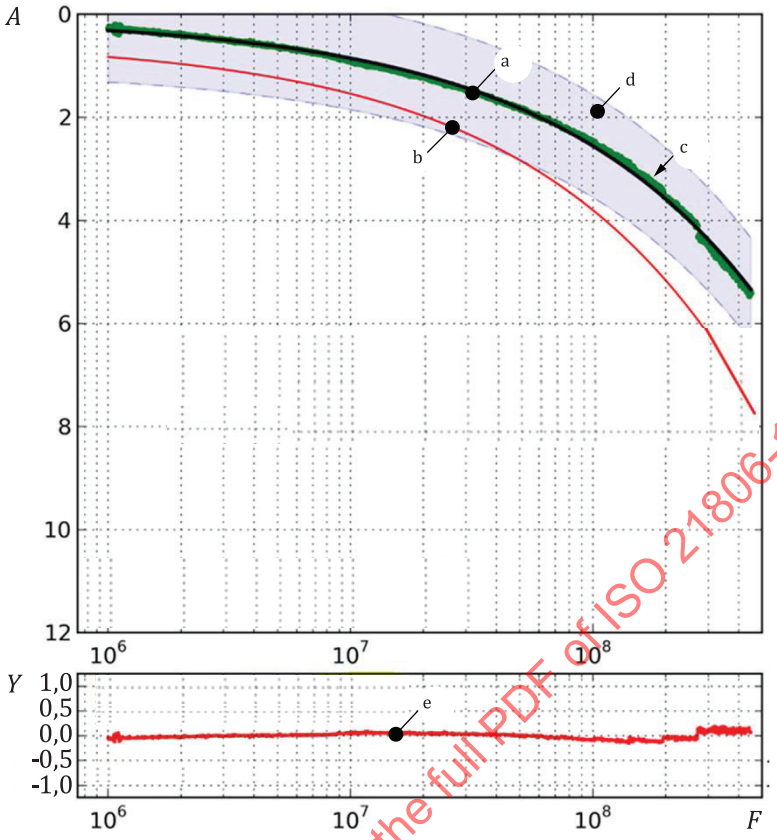
Figure 8 shows the attenuation conformance as specified in ISO 21806-10:2021, 9.4.1 and the residues for an IUT cable length of 15 m. Residue, in this context, refers to the deviation of a measured sample from the idealized curve for each frequency step.

A least square fitting algorithm fits the measured data to the given attenuation function, resulting in values for A_{DC_loss} and F_{skin}. The evaluated coefficients A_{DC_loss} < 0,07 dB and F_{skin} > 1,62 × 10^7 Hz/dB^2 are within the specified limits according to 8.4.2.

It is verified that:

— the measured samples are within the attenuation conformance corridor and

— the minimum and maximum values for residues, -0,16 dB and 0,19 dB, respectively, are within the limits specified in ISO 21806-10:2021, 9.4.1.



Key

A	attenuation [dB]
F	frequency [Hz]
Y	fit residue [dB]
a	Idealized attenuation curve approximating the measured performance of the IUT (attenuation function, with coefficients as determined by the fit).
b	MOST150 cPHY specification limits: idealized attenuation characteristic based on worst case coefficients A_{DC_loss} and F_{skin}.
c	Acquired data in frequency range 1 MHz to 450 MHz.
d	Attenuation conformance corridor.
e	Fit residue.

Figure 8 — Attenuation conformance

The A_{DC_loss} and F_{skin} coefficient limits restrict the allowed attenuation span. The attenuation conformance corridor ensures that the transfer characteristic of the IUT follows a transfer function of coaxial cables. As a result, signal passing such interconnect and being consecutively equalized (based on coaxial cable attenuation function) maintains a flatness of ±1 dB.

Particular coaxial interconnect configuration exhibits individual attenuation characteristics and is thus characterized by their respective individual A_{DC_loss} and F_{skin} coefficients. The values of those coefficients depend on the cable type used and the total length of each specific interconnect tested. Coaxial interconnect/segments with shorter length have lower attenuation and therefore lower A_{DC_loss} and larger F_{skin}. Interconnects with identical configuration can produce different coefficient sets.

Cable attenuation varies with temperature. This is mainly contributed by the temperature dependent conductance of the conductor's material (copper). Therefore, coefficients for a given interconnect vary over temperature.

Extrapolation of coefficient values for different cable lengths is defined in Formula (4) and Formula (5).

$$A_{\mathrm{DC\_loss}}(l) = \frac{A_{\mathrm{DC\_loss\_meas}}}{l_{\mathrm{IUT}}} \times l \tag{4}$$

where

$A_{\mathrm{DC\_loss}}$ represents the DC attenuation;

$A_{\mathrm{DC\_loss\_meas}}$ is the result of a fit on measured data;

l_{IUT} is the length of measured interconnect;

l is the desired length coefficients are extrapolated to.

$$F_{\mathrm{skin}}(l) = \frac{F_{\mathrm{skin\_meas}}}{l^2} \times {l_{\mathrm{IUT}}}^2 \tag{5}$$

where

F_{skin} represents skin effect losses;

$F_{\mathrm{skin\_meas}}$ represents skin effect losses as a result of a fit on measured data;

l_{IUT} is the length of measured interconnect;

l is the desired length coefficients are extrapolated to.

Table 2 shows an example using coefficient limits.

Table 2 — Example using coefficient limits

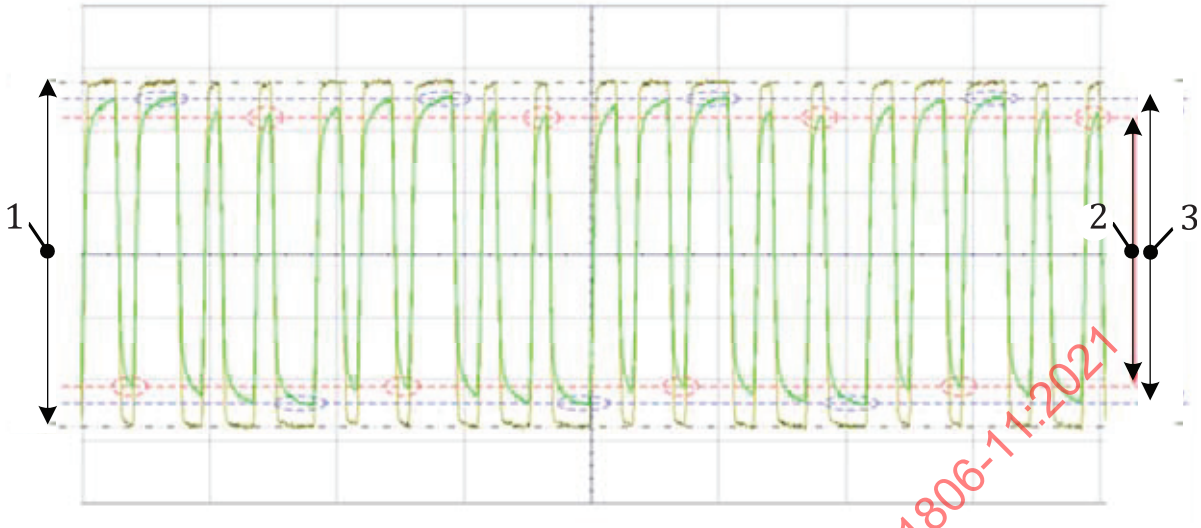
Measured	Extrapolated
l_{IUT}: 15 m $A_{\mathrm{DC\_loss\_meas}}$: 0,500 dB $F_{\mathrm{skin\_meas}}$: 9,2 × 10^6 Hz/dB^2	l_{IUT} extrapolated: 5 m $A_{\mathrm{DC\_loss}}(l)$: 0,167 dB $F_{\mathrm{skin}}(l)$: 8,28 × 10^7 Hz/dB^2
l_{IUT}: 5 m $A_{\mathrm{DC\_loss\_meas}}$: 0,167 dB $F_{\mathrm{skin\_meas}}$: 8,28 × 10^7 Hz/dB^2	l_{IUT} extrapolated: 15 m $A_{\mathrm{DC\_loss}}(l)$: 0,500 dB $F_{\mathrm{skin}}(l)$: 9,2 × 10^6 Hz/dB^2

8.4.5.5 Impact of attenuation on data signal

ISO 21806-10:2021, 9.4.1 specifies the attenuation characteristic of coaxial interconnect which follows a function of frequency. Therefore, the spectrum of a data signal being fed into such channel is attenuated in a non-uniform manner. Attenuation affects high frequencies more than low frequencies. In consequence, transition times decrease. Shorter pulses of the signal might not achieve full amplitude swing anymore. The effect is called intersymbol interference.

The graph in Figure 9 gives an example: the SP2 signal starts with uniform amplitude on all pulses (V_{ss2} in ISO 21806-10:2021, 9.3). The SP3 signal shows the resulting signal shape after passing the coaxial interconnect (typical coaxial cable, 15 m, same cable as used for analysis of link attenuation in 8.4.4).

Figure 9 shows the measurement of attenuation of coaxial interconnects.



Key

1 amplitude at SP2

2 minimum amplitude at SP3

3 maximum amplitude at SP3

Figure 9 — Measurement of attenuation of coaxial interconnects

8.5 RL of connectors and couplers

RL affects all types of connectors in the coaxial link, i.e. inline-couplers, harness connectors as well as ECU connectors. Testing of such connectors and couplers shall be performed in accordance with ISO 20860-2. The frequency range of interest for MOST150 cPHY is defined with 1 MHz to 450 MHz, which is only a sub-set of the requested bandwidth in ISO 20860-2.

8.6 Characteristic impedance of coaxial cable

Measurement of characteristic impedance of coaxial cables shall be performed according to EN 50289-1-11.

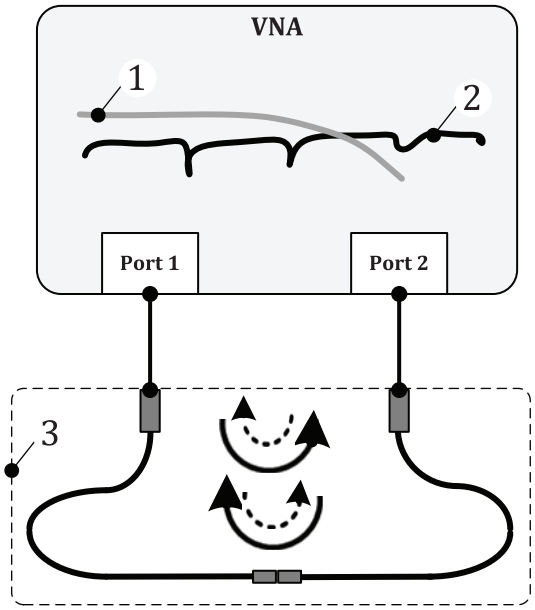
8.7 RL of coaxial interconnect

A coaxial interconnect is formed of one or more cables and the associated couplers and harness connectors. RL of a coaxial interconnect characterizes the frequency dependent signal reflection ratio, due to accumulated impedance mismatch throughout the whole length of that interconnect, measured at each of its ends.

RL shall be measured according to EN 50289-1-11 in the frequency range of 1 MHz to 450 MHz. ISO 21806-10 specifies neither the resolution nor the scale of the frequency axis for RL.

Typically, the RL measurement is combined with the attenuation measurement. The coaxial interconnect characteristic shall be measured in a 2-port arrangement. The VNA measures attenuation and reflection from both ports.

Figure 10 specifies the RL test set-up.

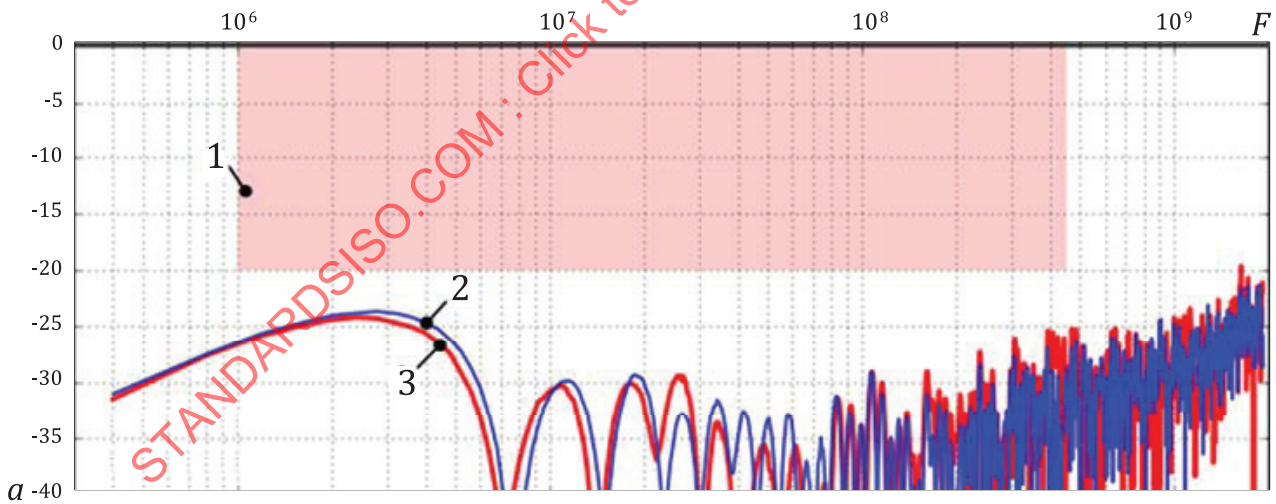


Key

1 attenuation
2 return loss
3 coaxial interconnect

Figure 10 — RL test set-up

Figure 11 shows an example plot of a measurement for evaluation of RL for a coaxial interconnect. RL is measured from both ports in both directions of the interconnect, resulting in S11 and S22.



Key

1 keep-out area
2 S22 scattering parameter
3 S11 scattering parameter
a amplitude [dB]
F frequency [Hz]

Figure 11 — Measurement for evaluation of RL of coaxial interconnects

8.8 RL of PCB interfaces

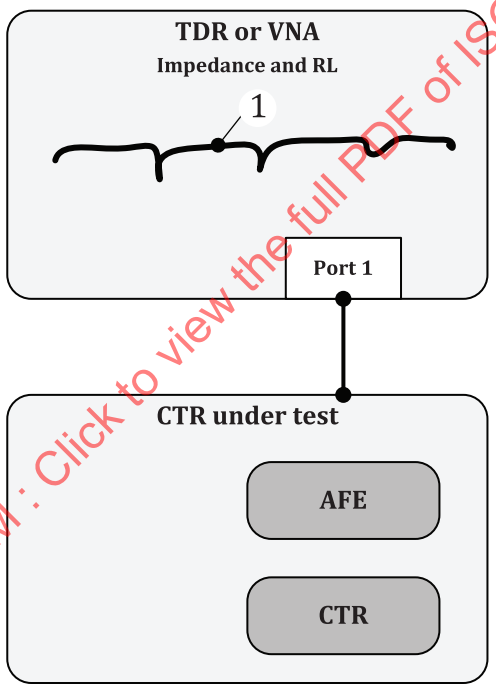
The connection of signals between a coaxial cable and a coaxial transceiver is realized on the PCB of the ECU. The circuitry, including passive components and PCB traces, is called analogue frontend. Also, this portion of the data link is expected to fit as close as possible to the characteristic line impedance of 50 Ω. Deviations in impedance matching cause reflections; RL is the ratio between transmitted and the reflected signal energy.

ISO 21806-10 specifies a limit-line in the frequency domain; the measurement however, may be performed in the time domain. The measurement set-up is a 1-port configuration, emitting a signal into a PCB interface (e.g. SP3 for simplex or combined SP2/3 in duplex) and measuring the reflected energy.

The TDR or VNA shall convert the result to magnitude in dB-scale and compare it with the limit-line. CTR is a coaxial transceiver as used in duplex applications; it is a synonym for CEC plus ECC for simplex applications.

For RL measurement of PCB interfaces the ECU is unpowered.

Figure 12 specifies the measurement set-up for evaluation of RL of PCB interfaces.

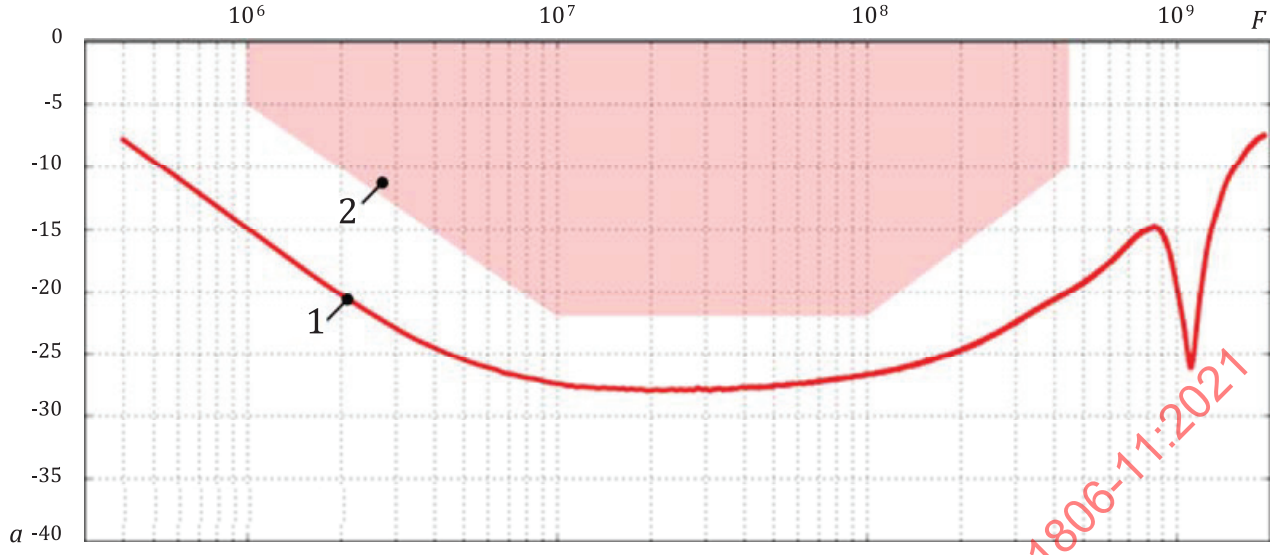


Key

1 impedance and return loss

Figure 12 — Measurement set-up for evaluation of RL of PCB interfaces

ISO 21806-10 specifies neither the resolution nor the scale of the frequency axis for RL. Figure 13 shows an example plot of a measurement of RL for a PCB interface.



Key

1 PCB interface
2 keep-out area
a amplitude [dB]
F frequency [Hz]

Figure 13 — Measurement for evaluation of RL of PCB interface

Time-domain reflection is another valuable method to evaluate the impedance characteristic of such PCB interfaces. The TDR sends a pulse into the IUT and measures response in magnitude and delay. The result usually is a plot of impedance over propagation time. For comparison with the specified limit-line (ISO 21806-10:2021, 9.4.2.3), TDR results are transferred to the frequency domain.

8.9 Stimulus creation for SP3

8.9.1 General

Evaluation of a coaxial receive portion means to apply worst-case signals to SP3 and to observe the response on the output of the receiver. In addition to signal quality testing, the activity detection conditions are tested. These tests need stimuli with lower amplitudes and different patterns than used for signal quality measurement.

The block-diagrams in 8.9.2 to 8.9.6 show simplified set-ups.

8.9.2 Pattern generator

A pattern generator is used to create MOST patterns, mainly for SP2. Such a pattern generator creates a signal that meets SP2 signal quality requirements (single-ended output, variation within extreme pulse shapes, variation with in extremes of timing distortion, adjustable output voltage).

Figure 14 shows the graphical element that represents a pattern generator.

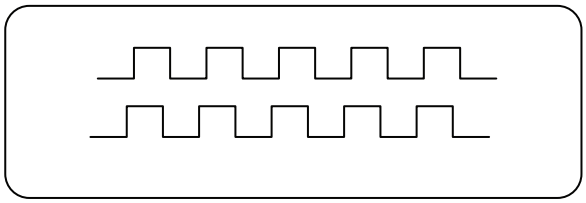


Figure 14 — Pattern generator

8.9.3 Arbitrary signal generator

An arbitrary signal generator is used to emulate coaxial signals, which includes signal variations as produced by a coaxial transmitter in combination with variations added by coaxial interconnects.

Figure 15 shows the graphical element that represents an arbitrary signal generator.

Figure 15 — Arbitrary signal generator

8.9.4 Attenuator

An attenuator is used in combination with the pattern generator or arbitrary signal generator to adjust the amplitude.

Figure 16 shows the graphical element that represents an attenuator.

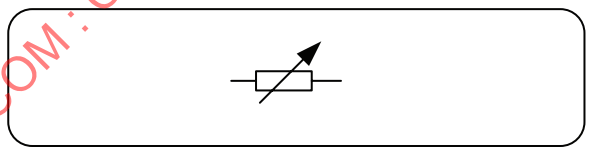


Figure 16 — Attenuator

8.9.5 Cable or analogue representation

A cable or analogue representation is used to emulate attenuation as produced by a coaxial interconnect. This can be either real cables with known transfer characteristics, analogue modules emulating such cable transfer characteristic or combinations of both.

Figure 17 shows the graphical element for a cable or analogue representation.

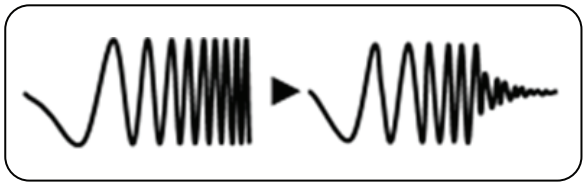


Figure 17 — Cable or analogue representation

8.9.6 Noise generator

A noise generator is used to generate crosstalk. Noise is added to the data signal to evaluate performance of a coaxial receiver under stress (duplex only).

Figure 18 shows the graphical element that represents a noise generator.

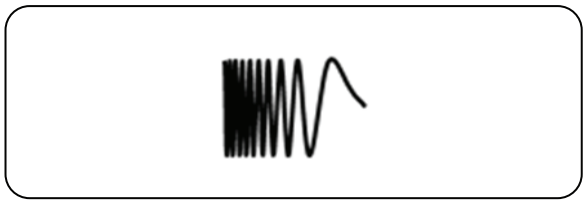


Figure 18 — Noise generator

8.9.7 Creating a stimulus for SP3 for simplex applications

Based on ISO 21806-10, the following impacts on signal quality at SP3 should be considered.

— Valid MOST data starts from SP2 (all variations permitted, e.g. minimum/maximum amplitude, transition times and jitter).

— Signal is attenuated when travelling through the interconnect.

— Some additional but minor losses occur at the interface cable to PCB (SP3).

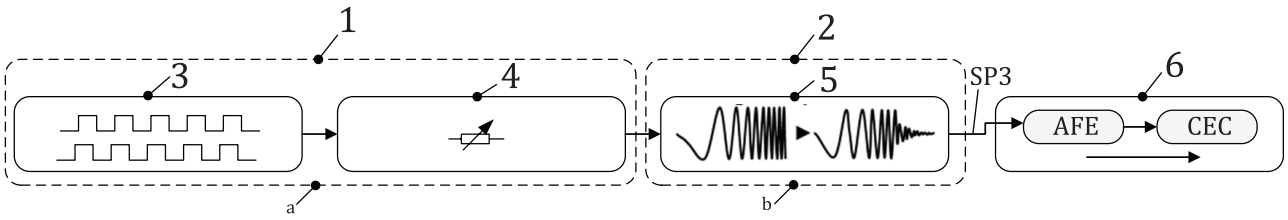
— For activity detection, patterns (lower frequency content) other than valid MOST patterns are used. Signal with lower amplitude or additional attenuation may be used for evaluating on-state/off-state thresholds.

There are three basic test set-ups which may be used to emulate the above listed influences and to stress an CEC under test. Table 3 specifies the configurations A and B (simplex applications).

Table 3 — Basic test set-ups for configuration A and B – Simplex applications

Cfg	ECC emulation (see key 1 of Figure 19)	Wire harness emulation (see key 2 of Figure 19)	CEport under test (see key 3 of Figure 19)
A	Pattern generator, signal conditioner, attenuator: — square wave, with frequency less than 10 kHz up to 75 MHz; — MOST150 cPHY stress pattern.	Frequency dependent attenuation: — use cables in various combinations, it requires pre-selected cables and components.	Apply stimulus to CEC. Check for sufficient/requested tolerance at CEC.
B	Pattern generator, signal conditioner, attenuator: — square wave, with frequency less than 10 kHz and up to 75 MHz; — MOST150 cPHY stress pattern.	Frequency dependent attenuation: — use specific circuitry, emulating cable characteristic with analogue filters; — a few characteristics may be combined on one PCB.	Apply stimulus to CEC. Check for sufficient/requested tolerance at CEC.

Figure 19 defines the simplex test set-ups A and B.



Key

1 ECC emulation
2 wire harness emulation
3 pattern generator
4 attenuator
5 cable or analogue representation
6 CEport under test
a Control on pattern for valid data and activity detection, amplitude, transition times, and output jitter.
b Control on frequency dependent attenuation, emulate various combinations of A_{DC_loss} and F_{skin}.

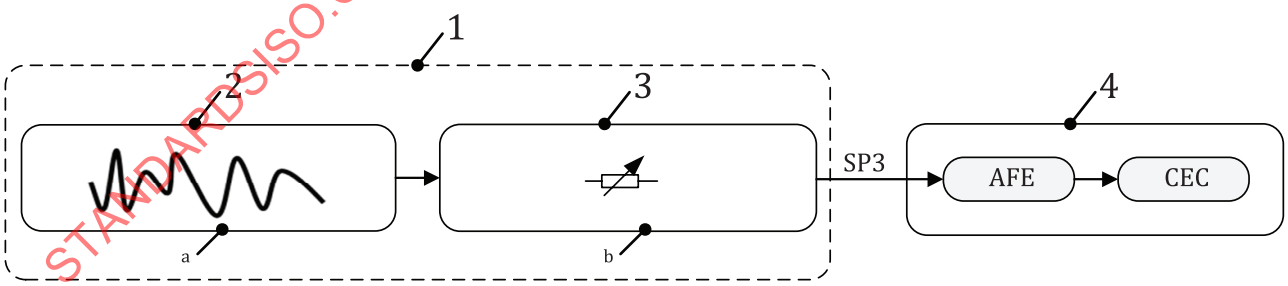
Figure 19 — Simplex test set-ups A and B

Table 4 specifies the configuration C (simplex applications).

Table 4 — Basic test set-up for configuration C – Simplex applications

Cfg	ECC and wire harness emulation (see key 1 of Figure 20)	CEport under test (see key 2 of Figure 20)
C	Using an arbitrary signal generator and attenuator – combining signal generation with cable emulation: — processing various patterns, including various signal conditions; — adding frequency dependent attenuation; — potentially, additional attenuation can be necessary.	---

Figure 20 defines the simplex test set-up C.



Key

1 ECC and wire harness emulation
2 arbitrary signal generator
3 attenuator
4 CEport under test
a Control on pattern for valid data and activity detection, amplitude, transition times, output jitter, frequency dependent attenuation, emulate various combinations of A_{DC_loss} and F_{skin}.
b Potentially, additional attenuation is necessary.

Figure 20 — Simplex test set-up C

Table 5 describes the advantages and disadvantages of suggested simplex test set-ups.

Table 5 — Advantages and disadvantages of suggested simplex test set-ups

Cfg	Advantage	Disadvantage
A, B	Wire harness/cable emulation can be reused in real network-links, multi node networks, qualification testing, end-of-line testing, etc.	Fixed structure, not adaptable, practically low number of test scenarios are applicable.
C	There is flexibility in generating multiple stress scenarios, easy adaptation for new configurations.	Not usable in real links, it cannot be reused in other test areas.

8.9.8 Creating a stimulus for SP3 for duplex applications

Based on ISO 21806-10, the following impacts on signal quality at SP3 should be considered.

— Valid MOST data is transmitted from the nodes on both sides of the link (all SP2 variations are permitted, e.g. minimum/maximum amplitude, transition times, and jitter); oppositional settings for both nodes are applied.

— Signals are attenuated when travelling through the interconnect.

— Some additional but minor losses occur at the interface cable to the PCB (SP3).

— Impedance mismatches along the link enable reflections. At the location of the mismatches, signal edges from both nodes cause reflections, which then overlay with the opposing signal. Amplitude of such crosstalk depends on the grade of impedance mismatch, amplitude and transition time of the triggering signal, as well as the location of the mismatch (attenuation due to the cable). Multiple reflections in one link may overlay constructively or destructively.

— For activity detection, other patterns (lower frequency content) than valid MOST patterns are used. Signal with lower amplitude or additional attenuation may be used for evaluating on-state/off-state thresholds. Activity detection is tested under presence of crosstalk.

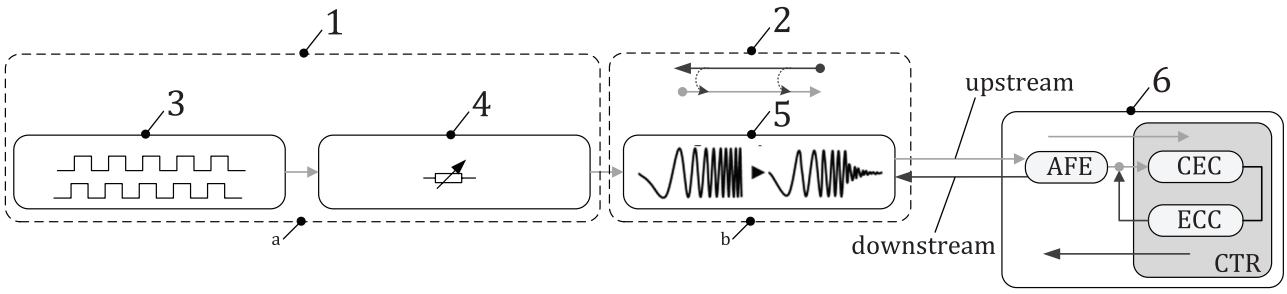
There are three basic test set-ups which may be used to emulate the above listed influences and to stress a CEC under test.

Table 6 specifies the configuration A.

Table 6 — Basic test set-up for configuration A – Duplex applications

Cfg	ECC emulation (see key 1 of Figure 21)	Wire harness emulation (see key 2 of Figure 21)	CEport under test (see key 3 of Figure 21
A	Pattern generator, signal conditioner, attenuator: — square wave, with frequency less than 10 kHz and up to 75 MHz; — MOST150 cPHY stress pattern.	Frequency dependent attenuation: — use cables in various combinations, it requires pre-selected cables and components; — impedance mismatches as exist, no possibility to control them.	ECC is actively transmitting downstream. Maximum amplitude and fast edges are used to cause maximum reflections.

Figure 21 defines the duplex test set-up A.



Key

1 ECC emulation (upstream)
2 wire harness emulation
3 pattern generator
4 attenuator
5 cable
6 CEport under test (upstream) and ECC emulation (downstream)
a Control on pattern for valid data and activity detection, amplitude, transition times, and output jitter.
b Control on frequency dependent attenuation, emulate various combinations of A_{DC_loss} and F_{skin}.

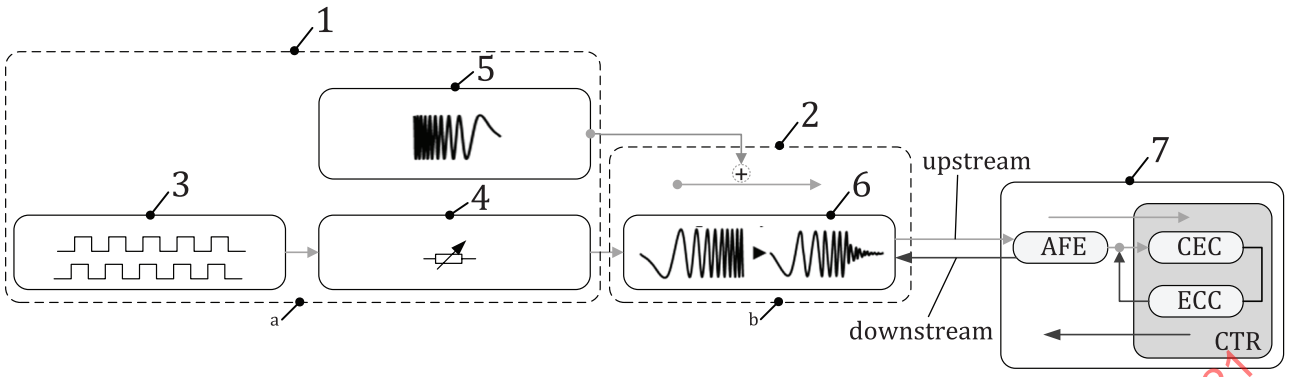
Figure 21 — Duplex test set-up A

Table 7 specifies the configuration B.

Table 7 — Basic test set-up for configuration B – Duplex applications

Cfg	ECC emulation (see key 1 of Figure 22)	Wire harness emulation (see key 2 of Figure 22)	CEport under test (see key 3 of Figure 22)
B	Pattern generator, signal conditioner, attenuator: — square wave, with frequency less than 10 kHz and up to 75 MHz; — MOST150 cPHY stress pattern.	Cable or analogue representation: — use specific circuitry, emulating cable characteristic with analogue filters. A few characteristics may be combined on one PCB; — add circuitry that allows overlaying noise/crosstalk, generated by another signal generator. Noise level shall be adjusted to levels corresponding with worst case RL figures in MOST150 cPHY; — noise signal shall be uncorrelated to the data stream in frequency and phase.	ECC is inactive. Crosstalk is emulated by the noise source.

Figure 22 defines the duplex test set-up B.



Key

1 ECC emulation (upstream)
2 wire harness emulation
3 pattern generator
4 attenuator
5 noise generator
6 analogue representation
7 CEport under test (upstream) and ECC emulation (downstream)
a Control on pattern for valid data and activity detection, amplitude, transition times, and output jitter.
b Control on frequency dependent attenuation, emulate various combinations of A_{DC_loss} and F_{skin}.

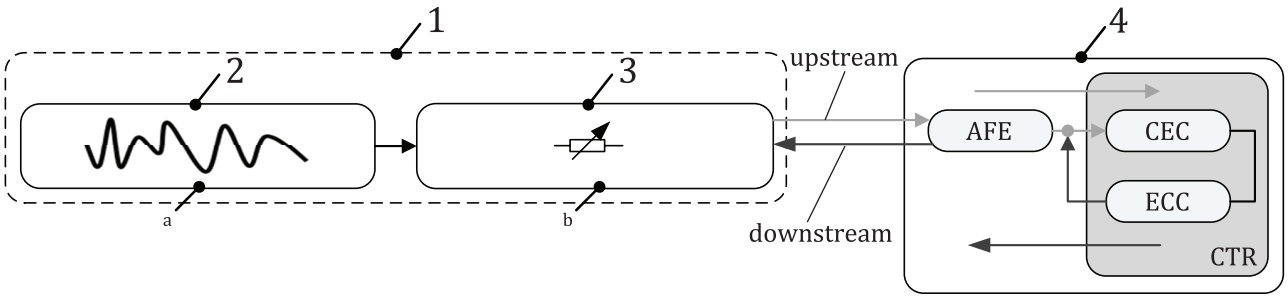
Figure 22 — Duplex test set-up B

Table 8 specifies the configuration C.

Table 8 — Basic test set-up for configuration C – Duplex applications

Cfg	ECC and wire harness emulation (see key 1 of Figure 23)	CEport under test (see key 2 of Figure 23)
C	Using an arbitrary signal generator, combining signal generation with cable emulation and crosstalk emulation: — processing various patterns, including various signal conditions; — adding frequency dependent attenuation; — adding amplitude noise; — potentially, additional attenuation can be necessary.	ECC is inactive. Crosstalk is implemented on test pattern.

Figure 23 defines the duplex test set-up C.



Key

1 ECC and wire harness emulation

2 arbitrary signal generator

3 attenuator

4 CEport under test

a Control on pattern for valid data and activity detection, amplitude, transition times, output jitter, frequency dependent attenuation, emulate various combinations of A_{DC_loss} and F_{skin}.

b Potentially, additional attenuation is necessary.

Figure 23 — Duplex test set-up C

Table 9 describes the advantages and disadvantages of the duplex test set-ups.

Table 9 — Advantages and disadvantages of the duplex test set-ups

Cfg	Advantage	Disadvantage
A	Wire harness/cable emulation can be re-used in real network-links, multi node networks, qualification testing, end-of-line testing, etc.	Fixed structure, not adaptable, practically low number of test scenarios applicable. Fixed crosstalk pattern, grade and location of impedance mismatches is fixed.
B	Wire harness/cable emulation can be reused in real network-links, multi node networks, qualification testing, end-of-line testing, etc. Limited reuse crosstalk generation, impacts signal in both directions.	Circuitry creates impedance mismatches, which are considered as a base impairment of the duplex link.
C	Flexibility in generating multiple stress scenarios, easy adaptation for new configurations.	Not usable in real links, no re-use in other test areas.

9 Measurement of phase variation

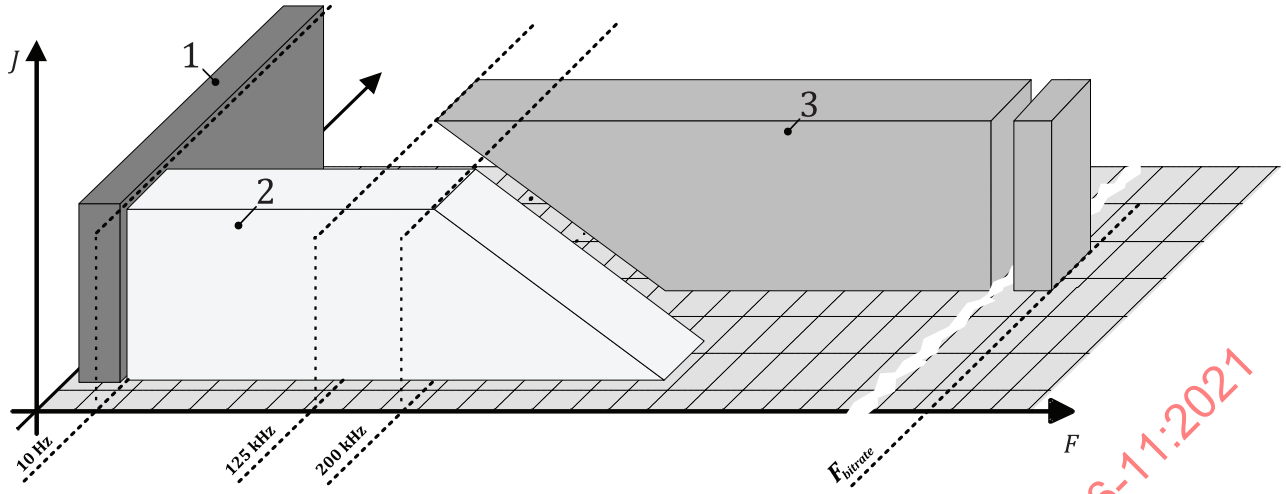
9.1 General

Phase variation is caused by data stream noise and distortion in the time domain. Based on spectral content of the variation, sub-categories of phase variation are defined. Table 10 specifies the measurement of phase variation.

Table 10 — Measurement of phase variation

Phase variation	Spectral limit
Wander	0 Hz to 10 Hz
Transferred jitter (TJ)	Jitter between 10 Hz and the limit given by the jitter filter.
Alignment jitter (AJ)	Jitter with spectral content above the limit given by the Golden PLL.

Figure 24 shows the sub-categories of phase variation.



Key

J	jitter
F	frequency
1	wander
2	transferred jitter
3	alignment jitter

Figure 24 — Sub-categories of phase variation

MOST is a synchronous network; therefore, separating TJ and AJ is necessary. Due to the coding scheme used, a clock signal is embedded in the data stream. The receive unit of a node recovers the clock used for sampling the received data stream from the data stream itself. The clock for sampling the output data of this node is derived from the recovered clock, which causes a certain phase correlation between the receive unit and the output section of a node.

Clock recovery is realized by using a phase locked loop (PLL). Using the PLL, phase variations can be tracked. Phase variation in a lower spectral range on an incoming data stream is compensated by aligning the clock's phase accordingly. Therefore, low-frequency jitter does not impact the data recovery. The clock for generating the output data, which is derived from the recovered input clock, is affected by the alignment process and may transfer phase variation from input to output.

High frequency jitter cannot be tracked by the PLL and leads to a temporary misalignment between sampling clock and input data, which limits the ability of error-free data recovery. A maximum misalignment (maximum alignment jitter) to be tolerated is defined with the eye masks for each specification point.

The dynamic characteristics of a PLL for a MOST node are covered by the physical layer specification with two definitions.

a) Golden PLL:

   The Golden PLL is given in the form of a transfer function representing a low-pass filter. The Golden PLL serves two purposes.

   1) It is used as a measurement tool for generating a time base, which is required for forming eye diagrams and determining AJ at each SP along a link. Based on the recovered UI clock an eye diagram is drawn. Eye masks, defined for each SP, give the limits for AJ respectively.

   2) It determines the behaviour of an MNC when jitter is applied to its input data. It marks the minimum capability of a PLL to track incoming phase variations. Jitter within the spectral range described by the low-pass filter is tracked by aligning the clock. Jitter beyond the spectral range described by the low-pass filter may lead to misalignment. The Golden PLL in

combination with the eye mask for SP4 receiver tolerance specifies the minimum AJ tolerance of an MNC's receive section.

b) Jitter filter:

The jitter filter is given in the form of a transfer function representing a low-pass filter. It serves two purposes.

1) It is used as a measurement tool for extracting transferred jitter (TJ) out of the total jitter.

2) Additionally, it determines the worst-case jitter transfer characteristic over an MNC. Jitter below the spectral range described by the low-pass filter may be tracked by a PLL. The data stream being generated by this MNC and sampled with the recovered clock may transfer this low-frequency part of the total jitter.

9.2 Measuring alignment jitter

Table 11 specifies a procedure for detecting AJ in a data stream. Oscilloscopes, appropriate for the jitter measurements, are digital sampling oscilloscopes (DSO) with deep sampling memory and special software modules for serial data analysis.

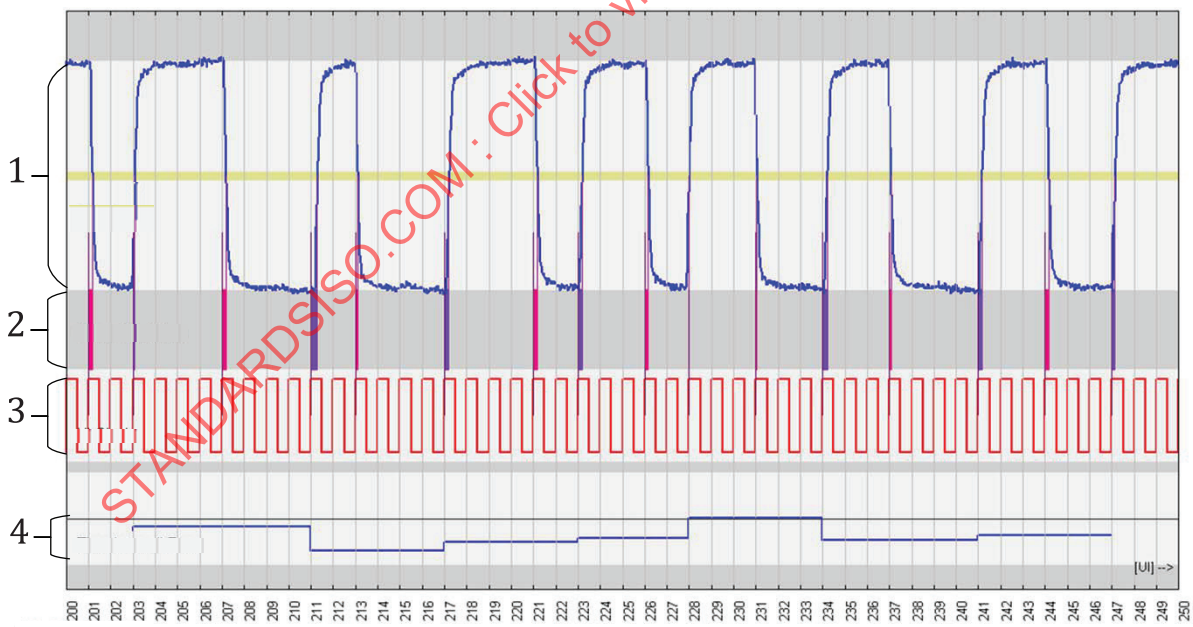
Table 11 — AJ measuring procedure

Action	Description
Acquiring a waveform	A probe (active differential or single-ended probe according to the SP under test) is connected to the IUT. The vertical scale is adjusted to achieve a sufficient vertical resolution. A sequence of the data stream ("waveform") is sampled into the oscilloscope's memory.
Clock recovery	The DCA-coded MOST150 data stream contains clock and data. In a first step, the oscilloscope shall extract the clock. Data pulses range from 2 UI to 6 UI yielding five different pulse widths (2 UI, 3 UI, 4 UI, 5 UI, and 6 UI). The required clock has a cycle time of 1 UI, which is twice the bit rate (i.e. for a ρ_{Fs} of 48 kHz, the bit rate is 147,45 Mbit/s and the UI clock is 294,91 MHz). A method of extracting the UI clock from a waveform is a mandatory function to be provided with the oscilloscope. In a first step, the recovered UI clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency. MOST150 specifies that the Golden PLL is applied on positive edges of the data stream only; the approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only.
Applying low-pass filter given by Golden PLL	Once a first derivate of the UI clock is approximated, there might still be phase differences between rising data edges and the recovered UI clock, called time interval errors. Applying the low-pass filter (given by the Golden PLL) to the sequence of consecutive time interval errors results in a filtered phase deviation sequence. This sequence represents the minimum capability of the MNC to track incoming phase variations by adjusting the phase of its sampling clock. In order to recover this sampling clock, phases of the first derivate of the UI clock shall be compensated by the sequence of filtered phase deviations. The resulting new UI clock, which is used for further calculations, now represents the base UI clock incorporated in the data stream, overlaid with a modulation in phase that follows phase variations in the data stream. The modulation capability is limited by the spectrum of the Golden PLL.
Calculating alignment jitter	Alignment jitter is the phase deviation between any edge of the waveform and the correlating transition of the recovered UI clock. Calculating the misalignment between clock and data for each data transition and drawing the successive phase deviations over runtime in a graph result in an "AJ track", which is the base for further evaluations. Calculating a frequency distribution out of the phase deviation results in an "AJ jitter histogram".

Table 11 *(continued)*

Action	Description
Drawing the eye diagram	For drawing the eye diagram, the waveform is sliced into intervals of 1 UI length aligned with the UI clock. The sliced waveform segments plus some overhead (i.e. 0,25 UI on both sides) are overlaid in one graph. As shown in Figure 25, each transition is drawn twice, first on the left side and second on the right side of the diagram. Therefore, the statistical distribution of transitions at the threshold level is identical on both sides of the eye diagram. Duty cycle distortion (DCD), if it exists, shifts the eye towards the mask. In Figure 26, logic 0 pulses are shorter than logic 1 pulses. The UI clock is referenced to rising edges, which causes the rising edges to be adjusted to the UI borders, while the falling edges are shifted by the amount of the DCD.
Pass/fail test using eye masks	Signal integrity shall be checked using eye masks. The masks are defined as keep-out areas; each violation is interpreted as a bit error. The masks are defined by hexagons with points A, B, C, D, E and F. Points A and D are limiting AJ while B, C, E, and F build constraints for amplitude and pulse shape.
Bit error rate	The requested BER of 10^{-9} is represented by an eye diagram showing at least 10^9 bits without violation of the mask. 1 bit is represented in 2 UI. Therefore, at least 2×10^9 samples are required. Alternatively, statistical methods for accelerated testing of BER are acceptable. Selection of a method for extrapolation and definition of the required database to be measured for extrapolation is the responsibility of the user.

Figure 25 shows the example 1 of measuring alignment jitter. The UI clock is fitted in frequency and phase to the waveform. Remaining phase deviations are marked in the diagram. Phase deviations for rising edges are shown in the time interval error graph.



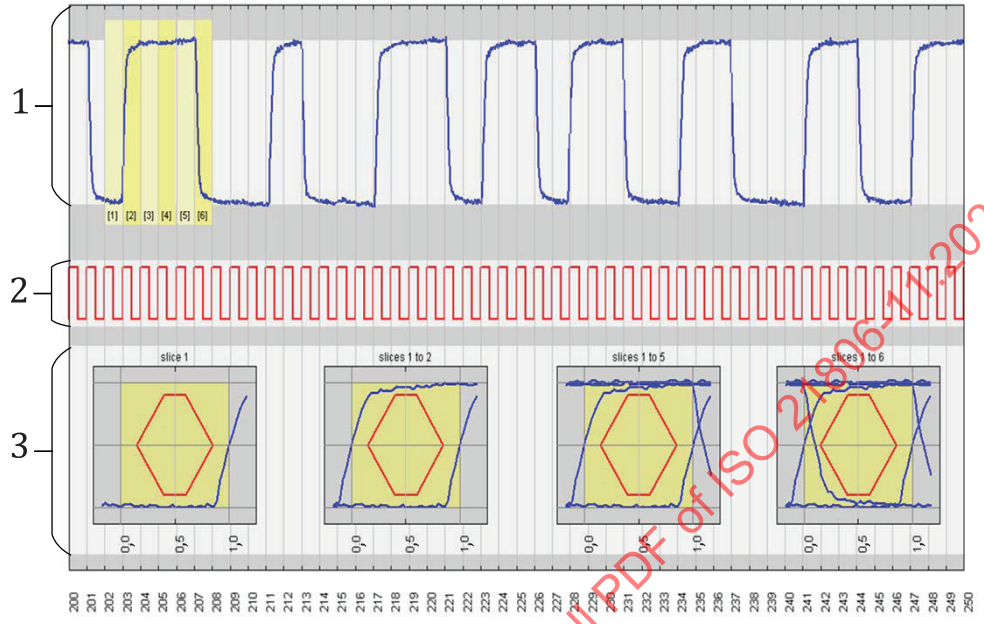
Key

1 waveform input signal
2 phase deviation
3 UI clock
4 time interval error

Figure 25 — Example 1 of measuring alignment jitter

NOTE In many oscilloscopes, visualization of the recovered UI clock is not possible.

Figure 26 shows the example 2 of measuring alignment jitter. The sliced waveform segments are marked in the waveform graph. The segments are overlaid in eye diagrams.



Key

1 waveform input signal
2 UI clock
3 eye diagrams

Figure 26 — Example 2 of measuring alignment jitter

9.3 Measuring transferred jitter

Table 12 specifies a procedure of determining TJ in a measured data stream.

Table 12 — Measuring transferred jitter

Action	Description
Acquiring a waveform	For this measurement, the maximum available sampling memory of the oscilloscope shall be used. A probe (active differential or single-ended probe according to the SP under test) is connected to the IUT interface. The vertical scale is adjusted to achieve a sufficient vertical resolution; see 8.1 and 8.3. A sequence of the data stream, which is referred to as waveform, is sampled into the oscilloscope's memory. TJ is defined in the spectrum from 10 Hz (beyond wander) to 200 kHz. The determination of this jitter is limited by the size of memory of the oscilloscope.

Table 12 *(continued)*

Action	Description
Clock recovery	Similar to the AJ measurement procedure, the clock shall be extracted. Clock separation is provided by an oscilloscope internal function. Similar to the AJ measurement procedure, the recovered UI clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency. The approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only. In contrast to the AJ measurement procedure, a PLL functionality for tracking phase variations is basically not necessary. Small deviations in the detected BR might grow to a significant phase mismatch over the length of the acquired waveform and, therefore, affect further results. To enable a robust measurement procedure, it is tolerable to apply a PLL with lowest possible bandwidth (as close as possible to 10 Hz).
Extracting transferred jitter	Jitter is the phase deviation between an edge of the waveform and the correlating transition of the recovered UI clock. For transferred jitter, only phase variations coming with rising edges of the waveform are relevant because only these deviations are tracked by the PLL and impact the recovered clock's phase. Calculating the misalignment between clock and data for rising edges and drawing the successive phase deviations over runtime in a graph result in a "jitter track". Successive phase deviations appear in pulse time intervals (2 UI, 3 UI, 4 UI, 5 UI, and 6 UI), which correspond to the theoretical maximum jitter frequencies up to 150 MHz. With respect to the focused spectral range 10 Hz to 200 kHz, it is acceptable to reduce the amount of jitter values by skipping samples in regular intervals. The reduction might be helpful for accelerating the measurement process. In the next step, this jitter track (optionally reduced) shall be low passed, using the transfer function given with the jitter filter definition, which results in the "filtered jitter".
Calculating transferred jitter	Transferred jitter is calculated by accumulating the phase deviations of the filtered jitter by using the root-mean-square method (v_{RMS}) as specified in Formula (6). If the spectrum of the filtered jitter contains values below 10 Hz (e.g. caused by a constant phase mismatch between clock and data), the standard deviation as specified in Formula (7) may be calculated instead of the v_{RMS}.

$$v_{RMS} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} v_i^2} \tag{6}$$

where

v_{RMS} is the transferred jitter, calculated using the root-mean-square method;

N is the number of samples;

i is the index of summation;

v is the phase deviation.

$$S_{Dev} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} \left(v_i - v_{mean}\right)^2} \tag{7}$$

where

S_{Dev} is the standard deviation;

N is the number of samples;

i is the index of summation;

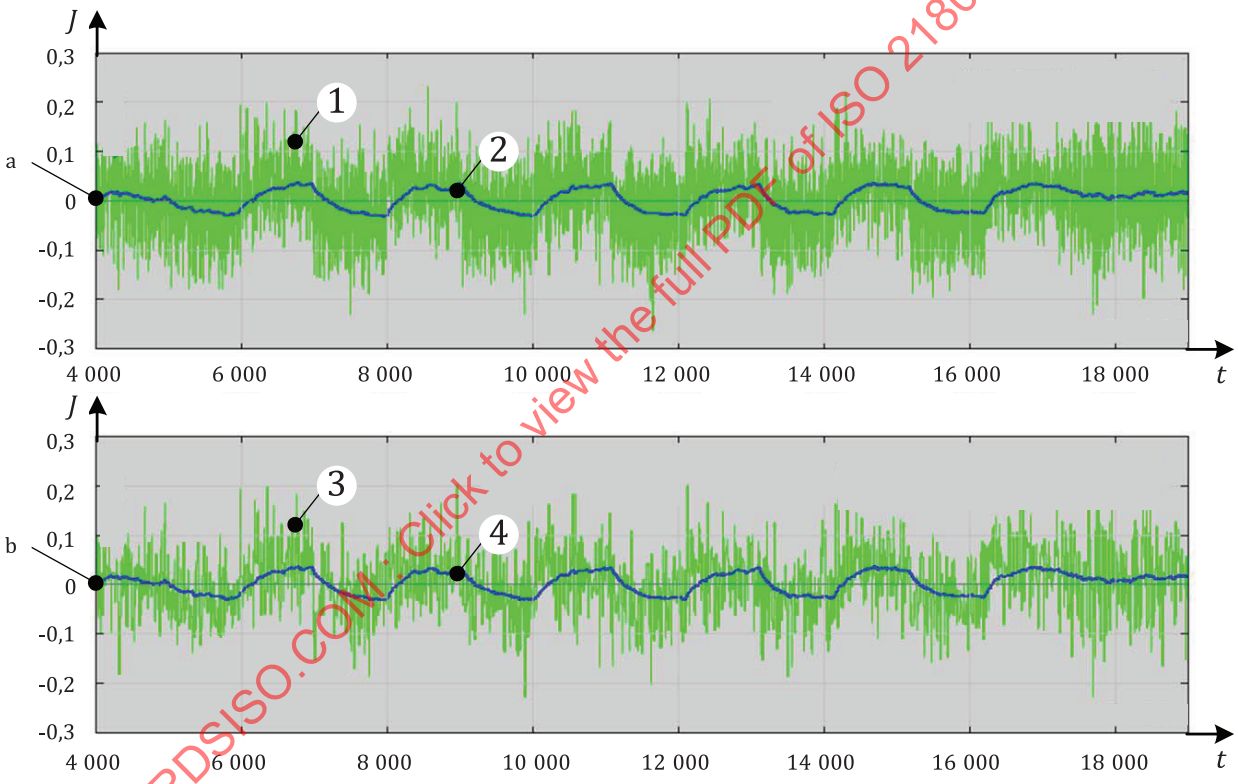
v is the phase deviation;

v_{mean} is the mean (average) phase deviation.

EXAMPLE of measuring transferred jitter:

— Figure 27 upper graph: successive phase deviations are shown over runtime (jitter unfiltered), weighting with the jitter filter leads to the low-passed version (jitter filtered);

— Figure 27 lower graph: successive phase deviations but reduced by factor 10 are shown over runtime (jitter unfiltered), weighting with the jitter filter leads to the low-passed version (jitter filtered).



Key

J jitter [UI]

t time [UI]

1 jitter unfiltered (green signal)

2 jitter filtered (blue signal)

3 jitter unfiltered, reduced by 1/10 (green signal)

4 jitter filtered, reduced by 1/10 (blue signal)

a Successive phase deviations are shown over runtime (jitter unfiltered), weighting with the jitter filter leads to the low-passed version (jitter filtered).

b Successive phase deviations but reduced by factor 10 are shown over runtime (jitter unfiltered), weighting with the jitter filter leads to the low-passed version (jitter filtered).

Figure 27 — Example of measuring transferred jitter

10 Test set-ups

10.1 General

This subclause specifies measurement set-ups, suggested to determine link quality parameters as specified in ISO 21806-10. The focus is set on measurement of specific characteristics of the MOST150 cPHY, while evaluation of LVDS-based signal parameters is not discussed here. Suggested set-ups are targeting evaluation of pulse shape and timing distortion at the output of a coaxial transmitter and timing distortion on a data signal after passing a coaxial receiver.

The following applies:

— pulse shape includes amplitudes and transition times;

— timing distortion means all kind of jitter, visible at the crossing of signal edges with regard to the respective threshold;

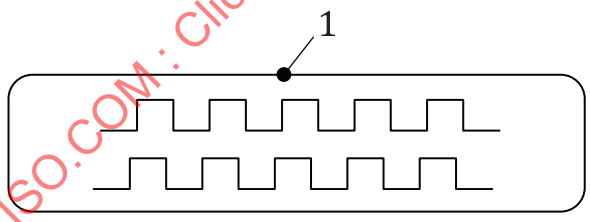
— the eye mask measurement used for evaluation of alignment jitter combines pulse shape and timing distortion. The additionally specified pulse shape parameters are more stringent and also more accurate. Therefore, eye mask measurement does not replace the discrete evaluation of all other parameters.

The set-ups are selected based on the operation mode, simplex or duplex. A set-up is adapted to the chosen configuration of the application, using a standalone or an integrated transceiver component.

10.2 Graphical symbols and descriptions

10.2.1 Pattern generator SP1

Figure 28 shows the graphical representation of a pattern generator, mainly for SP1. Such a pattern generator shall be able to create a signal following the SP1 signal quality requirements (LVDS, variation within extreme pulse shapes, variation with in extremes of timing distortion).



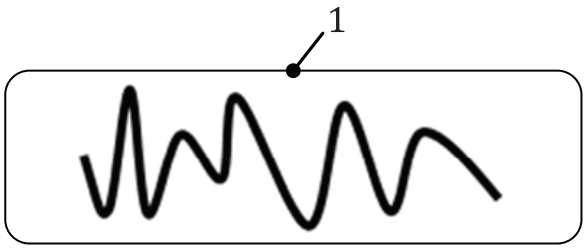
Key

1 pattern generator

Figure 28 — Pattern generator

10.2.2 SP3 stimulus

Figure 29 shows the graphical representation of the SP3 stimulus. This stimulus is an emulation of coaxial signals. The emulation generates a signal following the SP2 requirements (including all tolerable variations), or a signal resembling that of a coaxial transmitter in combination with a coaxial interconnect as described in 8.9.



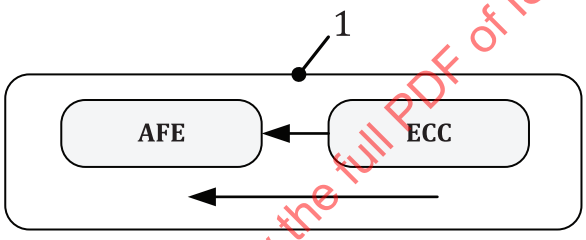
Key

1 SP3 stimulus

Figure 29 — SP3 stimulus

10.2.3 Standalone simplex ECport under test

Figure 30 shows the graphical representation of a standalone simplex ECport under test which includes the coaxial transmitter component ECC and the analogue frontend, both applied on a PCB. This symbol is used for standalone transceiver chips in simplex mode.



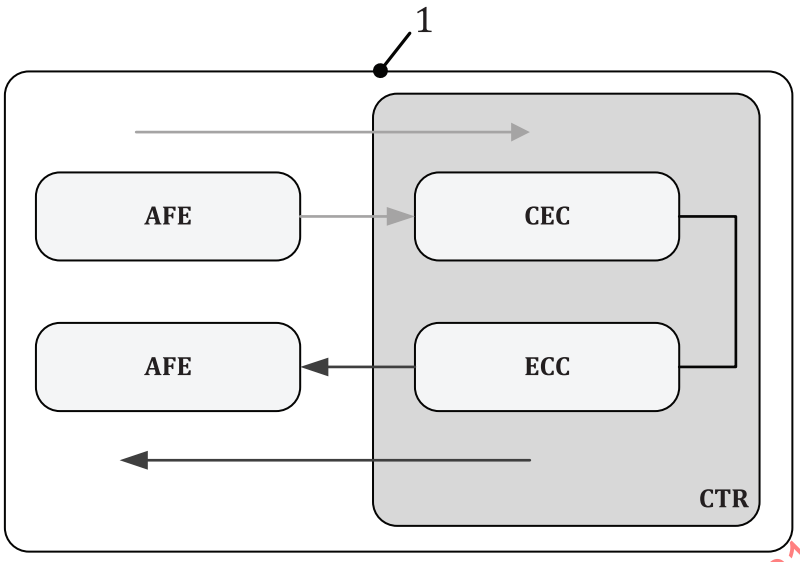
Key

1 ECport under test

Figure 30 — Standalone simplex ECport under test

10.2.4 Integrated simplex ECport under test

Figure 31 shows the graphical representation of an integrated simplex ECport under test which includes the coaxial transmitter component ECC, the coaxial receiver component CEC, and the analogue frontends, all applied on a PCB. The focus of evaluation is set on ECport performance. This symbol is used for integrated transceivers in simplex mode.



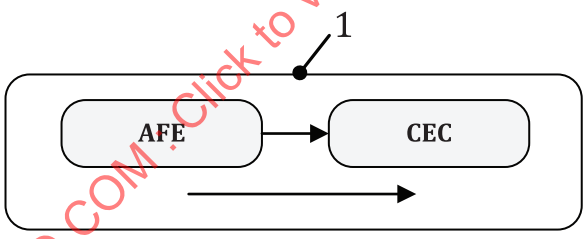
Key

1 ECport under test

Figure 31 — Integrated simplex ECport under test

10.2.5 Standalone simplex CEport under test

Figure 32 shows the graphical representation of a simplex CEport under test which includes the coaxial receiver component CEC and the analogue frontend, both applied on a PCB. This symbol is used for standalone transceiver chips in simplex mode.



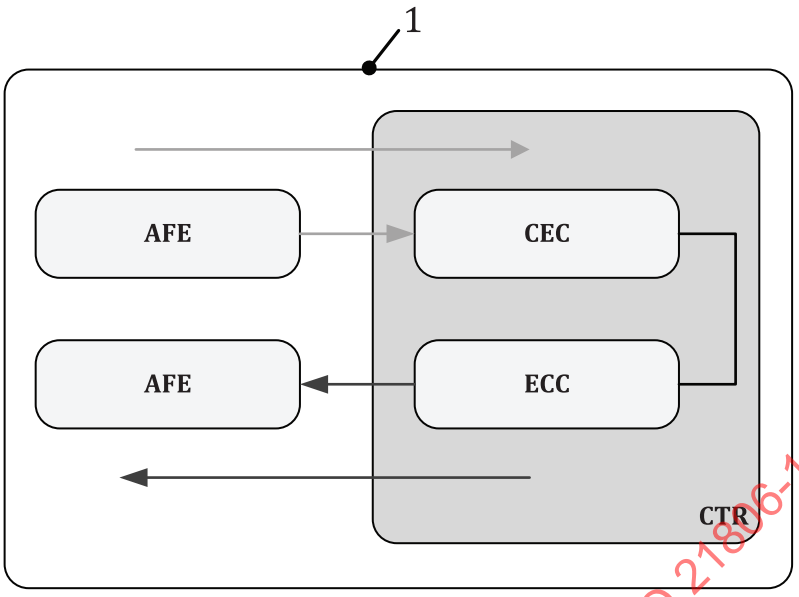
Key

1 CEport under test

Figure 32 — Standalone simplex CEport under test

10.2.6 Integrated simplex CEport under test

Figure 33 shows the graphical representation of an integrated simplex CEport under test which includes the coaxial receiver component CEC, the coaxial transmitter component ECC, and the analogue frontends, all applied on a PCB. The focus of evaluation is set on CEport performance. This symbol is used for integrated transceivers in simplex mode.



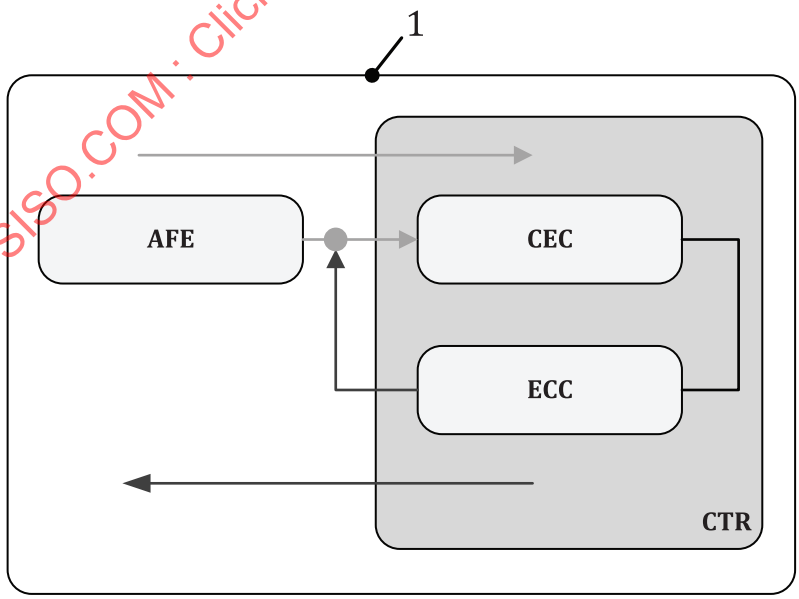
Key

1 CEport under test

Figure 33 — Integrated simplex CEport under test

10.2.7 Duplex ECport under test

Figure 34 shows the graphical representation of a duplex ECport under test which includes the coaxial transmitter component ECC, the coaxial receiver component CEC, and the analogue frontend, all applied on a PCB. The focus of evaluation is set on ECport performance. This symbol is used for transceivers in duplex mode.



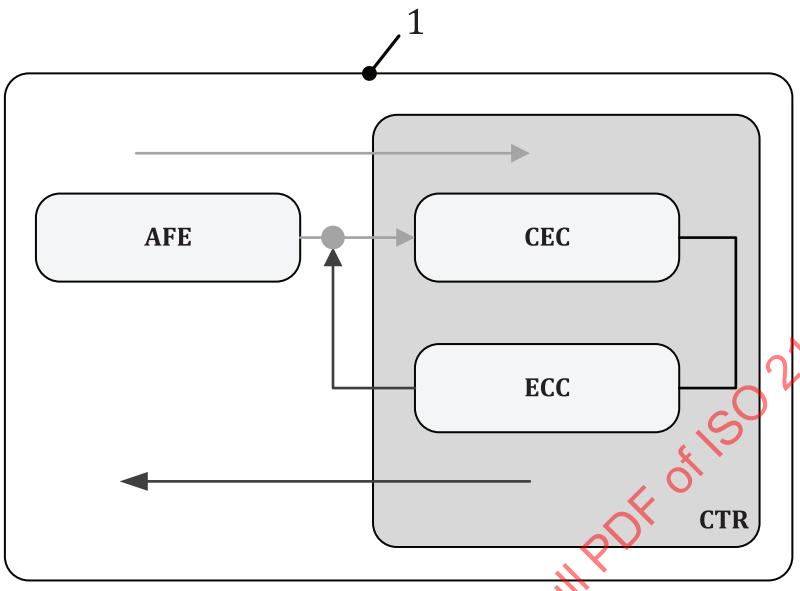
Key

1 ECport under test

Figure 34 — Duplex ECport under test

10.2.8 Duplex CEport under test

Figure 35 shows the graphical representation of a duplex CEport under test which includes the coaxial receiver component CEC, the coaxial transmitter component ECC, and the analogue frontend, all applied on a PCB. The focus of the evaluation is set on CEport performance in duplex mode. This symbol is used for transceivers in duplex mode.



Key

1 CEport under test

Figure 35 — Duplex CEport under test

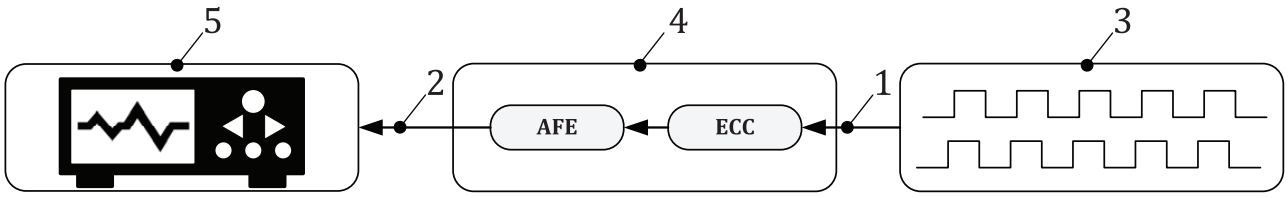
10.3 Set-ups for dual simplex

10.3.1 General

In dual simplex mode, signals are transmitted on separate cables per signalling direction.

10.3.2 SP2 signal quality measurement for simplex

An ECC realized as a standalone component offers a differential input interface in LVDS technology at SP1 and a single-ended output interface at SP2. Signal quality as a response to the input signal and operating conditions can be measured at SP2. The test set-up shown in Figure 36 can be used for evaluation of transition times, steady state amplitude and jitter.

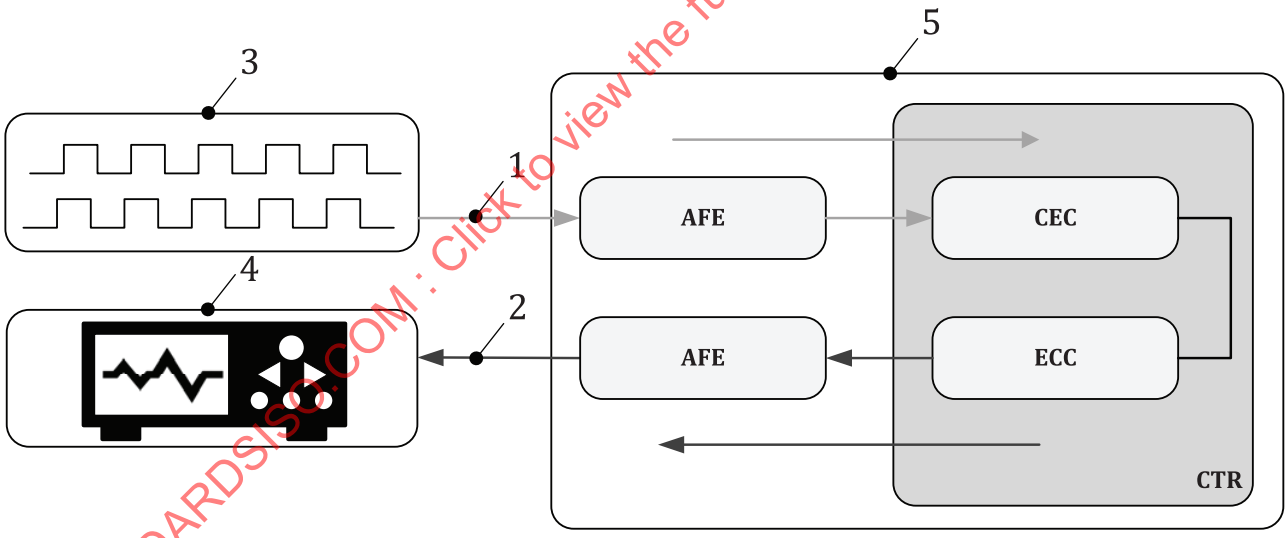


Key

1 SP1
2 SP2
3 pattern generator
4 ECport under test
5 oscilloscope

Figure 36 — SP2 signal quality measurement set-up for simplex and standalone transceiver

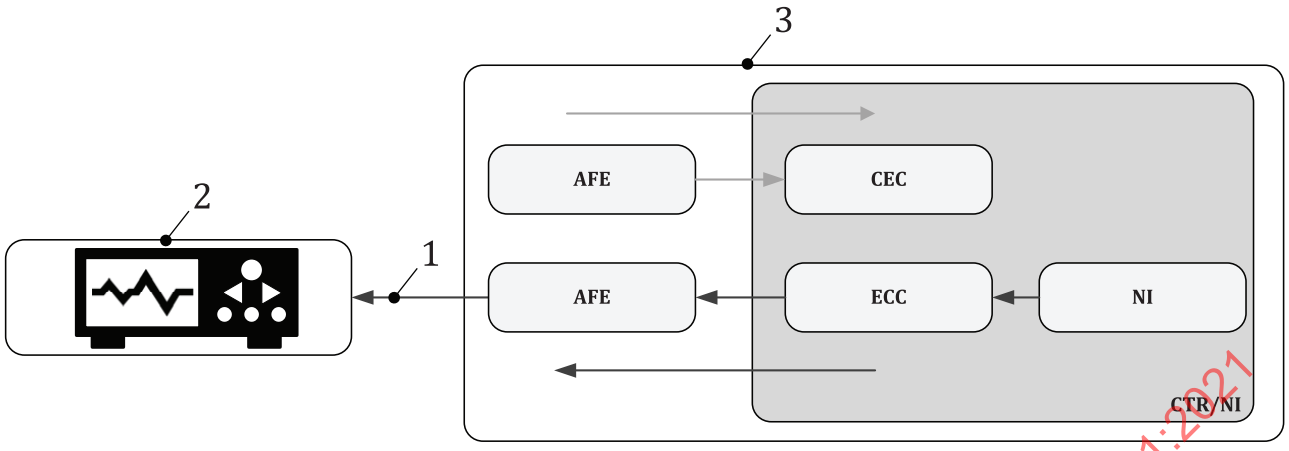
As specified in ISO 21806-10, integrated transceivers do not necessarily offer direct access to SP1. The ECC input signal can be stimulated by making use of the bypass. As shown in Figure 37, in bypass mode the CEC output signal is retransmitted on the ECC. An ECC provides a reshaping of the output signal but no retiming. Therefore, the ECC output signal provides the opportunity on direct evaluation of transition times and steady state amplitude. Timing distortion measured at SP2 includes contribution from of CEC and ECC. A reference of ECC performance shall be measured upfront and the result can be compensated for the ECC impact. An example for such reference measurement is shown in Figure 38.



Key

1 SP3
2 SP2
3 pattern generator
4 oscilloscope
5 ECport under test

Figure 37 — SP2 signal quality measurement set-up for simplex and integrated transceiver



Key

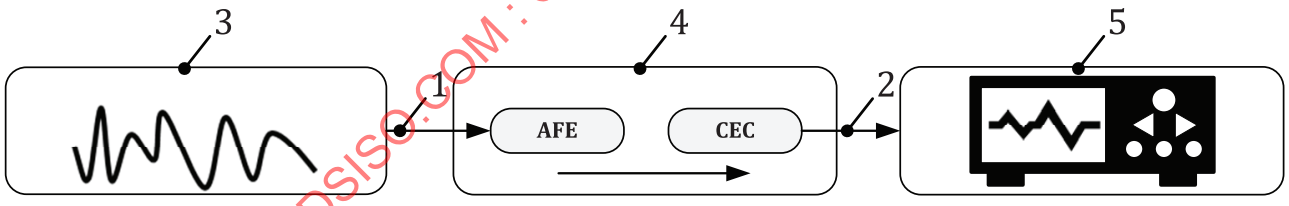
1 SP2
2 oscilloscope
3 ECport under test

Figure 38 — SP2 jitter measurement set-up for simplex and integrated transceiver, reference with data from MNC

10.3.3 SP4 jitter measurement (AJ and TJ) for simplex

As discussed in 8.9, there are various influences on a transmission channel that degrade signal quality of an input signal at SP3. Such impacts as well as the operating conditions of a coaxial receiver determine the signal quality at SP4.

A CEC realized as a standalone component exhibits an output interface in LVDS technology. Signal quality as a response to SP3 input stimuli and operating conditions can be measured as jitter (AJ and TJ). A test set-up in simplex operation is shown in Figure 39.



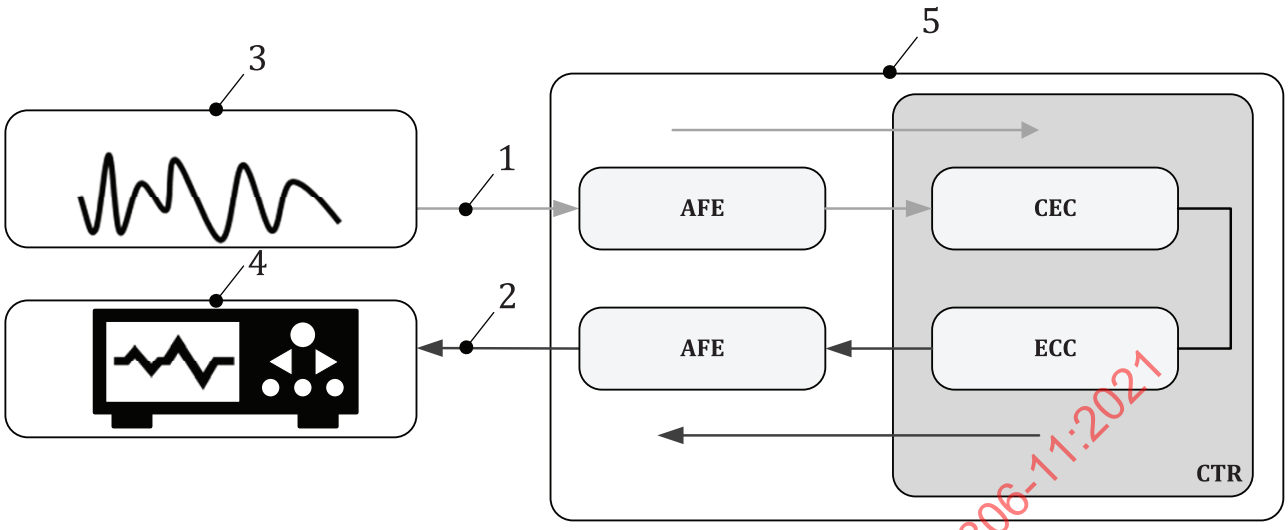
Key

1 SP3
2 SP4
3 SP3 stimulus
4 CEport under test
5 oscilloscope

Figure 39 — SP4 jitter measurement for simplex and standalone transceiver

For integrated transceiver as specified in ISO 21806-10, the CEC output signal can be accessed making use of the bypass. The CEC output is retransmitted on the ECC. This provides a reshaping of the ECC output signal but no retiming. The measured signal then includes timing distortion of the CEC plus the ECC. A reference of ECC performance shall be measured upfront and the result can be compensated for the ECC impact.

Figure 40 defines the SP4 jitter measurement for simplex and with integrated transceiver.



Key

1 SP3
2 SP2
3 SP3 stimulus
4 oscilloscope
5 CEport under test

Figure 40 — SP4 jitter measurement for simplex and with integrated transceiver

10.4 Set-ups for duplex

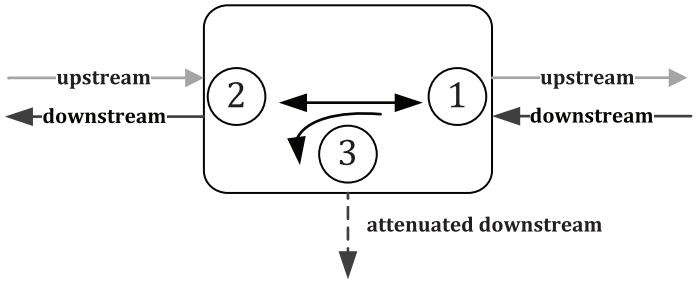
10.4.1 General

In duplex mode, signals are transmitted in both directions over the same cable. Upstream and downstream signals are overlaying each other. For unification and simplification, the following test set-ups are showing the ECC under test to drive the downstream path, while incoming signals are always fed from the upstream path.

10.4.2 Directional couplers

Signal quality measurements in duplex links are performed using directional couplers. The directional coupler provides three terminals. Two of them offer a bidirectional transmit path; a third terminal provides a branch from one of the other two terminals. The coupler itself is a non-ideal component and, therefore, has an impact on the signals.

Figure 41 shows a directional coupler with three terminals (1, 2, 3). Upstream and downstream signals are applied to terminals 1 and 2. An attenuated version of downstream is produced at terminal 3.



Key

1 terminal 1
2 terminal 2
3 terminal 3

Figure 41 — Directional coupler

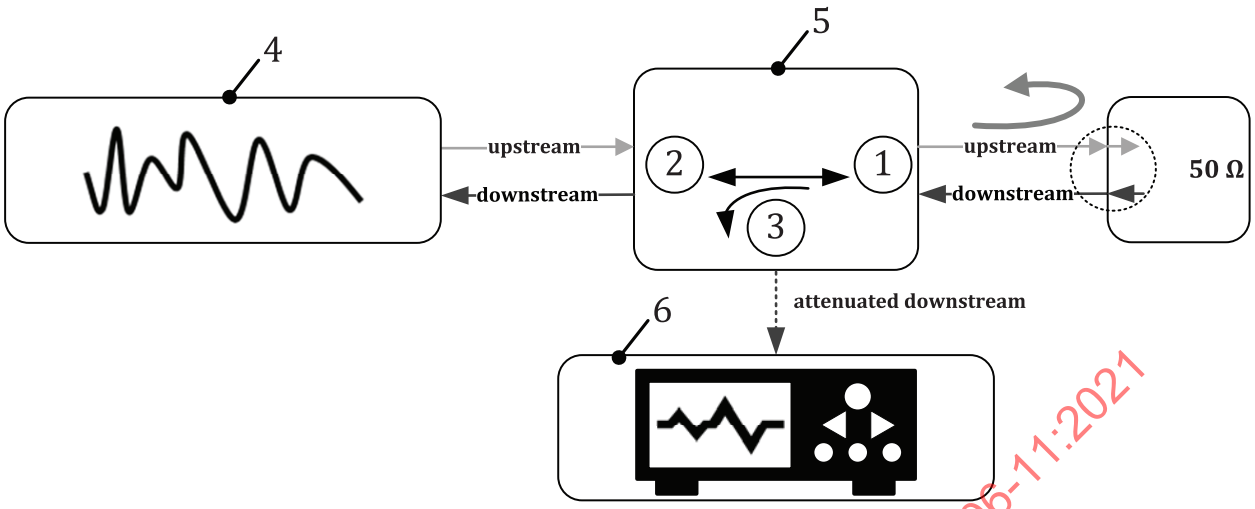
Table 13 describes the signal impairments due to directional coupler.

Table 13 — Signal impairments due to directional coupler

Impairment	Effect
Insertion loss	The transmit path between terminal 1 and terminal 2 attenuates both signals of the duplex link.
Coupling loss	The signal from terminal 1 to terminal 3 provides an attenuated copy of the signal on terminal 1.
RL	The impedances on the terminals of the coupler may deviate from the optimal value of 50 Ω. This creates impedance mismatches with the connected components and therefore causes losses and reflections.
Directivity	A crosstalk path between the signal path from terminal 2 to terminal 1 and from terminal 1 to terminal 3 might exist.

All the listed impairments are functions of frequency. The grade of attenuation and imperfection depends on the chosen product. Depending on the chosen product, not all might end up in measurable distortion, de-embedding of known impairments is recommended.

A method to evaluate crosstalk caused by a directional coupler is depicted in Figure 42.



Key

1 terminal 1
2 terminal 2
3 terminal 3
4 SP3 stimulus
5 directional coupler
6 oscilloscope

Figure 42 — Crosstalk caused by directional coupler, measured with ideal 50 Ω

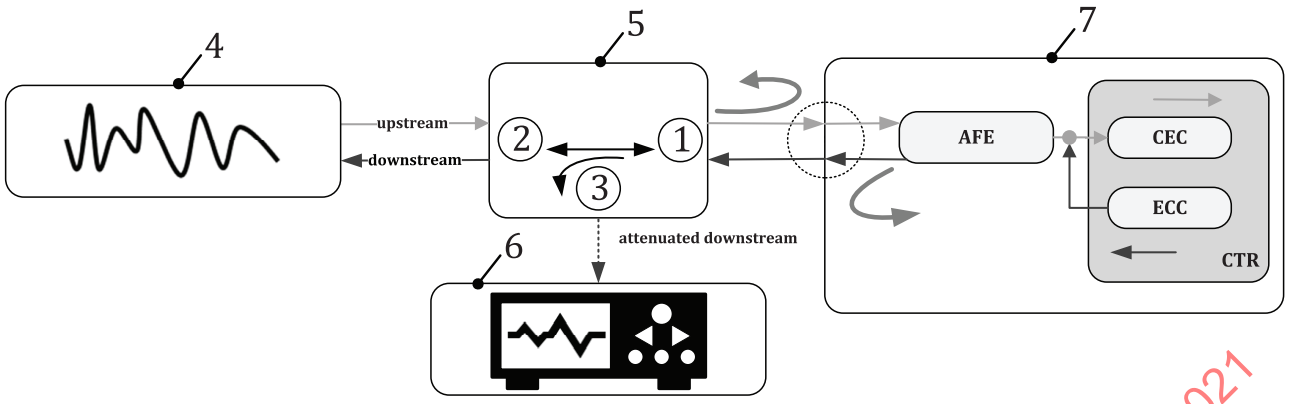
NOTE In a test set-up, where an IUT is connected instead of the ideal 50 Ω termination, it is possible that the impedance of the IUT deviates from 50 Ω (see ISO 21806-10). Therefore, the total impedance mismatch can be larger or smaller as seen in the aforementioned set-up.

Reflections are triggered by signal edges coming from both sides of the mismatch. In a duplex link, two potential causes of reflections exist.

— The SP3 stimulus in the upstream path creates reflections, which are overlaying with the downstream signal. This affects the out-coupled signal (attenuated downstream). This might compromise parameter performance measured with the oscilloscope.

— The ECC output signal (downstream) causes reflections, which are overlaying with the upstream signal inside the IUT. This degrades the input signal into the CEC. This might compromise signal quality presented to the CEC input and affect the response of activity detection circuitry inside the transceiver.

Figure 43 shows the crosstalk caused by directional coupler, in real set-up 1.



Key

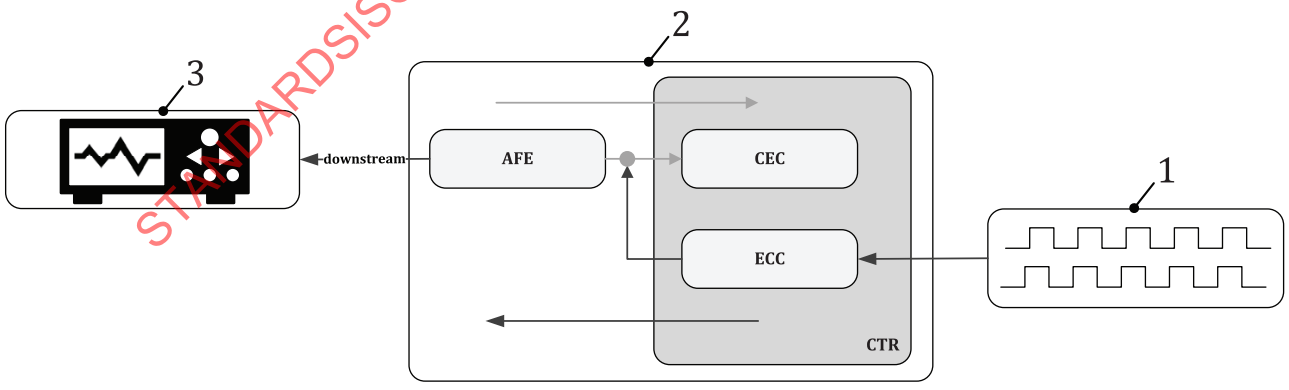
1 terminal 1
2 terminal 2
3 terminal 3
4 SP3 stimulus
5 directional coupler
6 oscilloscope
7 IUT

Figure 43 — Crosstalk caused by directional coupler, in real set-up 1

10.4.3 SP2 signal quality measurement for duplex

In duplex mode, signals are transmitted in both directions over the same cable. Upstream and downstream signals are overlaying each other. The following test set-ups are showing the ECC under test to drive the downstream path, while incoming signals are fed from upstream path.

Duplex transceivers realized as standalone component, provide differential input interfaces in LVDS technology. Evaluation of the ECC's signal quality can be done without the presence of an upstream signal. The set-up is shown in Figure 44. From a function point of view, this set-up is identical with the set-up shown in Figure 36. The test set-up can be used for evaluation of transition times, steady state amplitude and jitter.

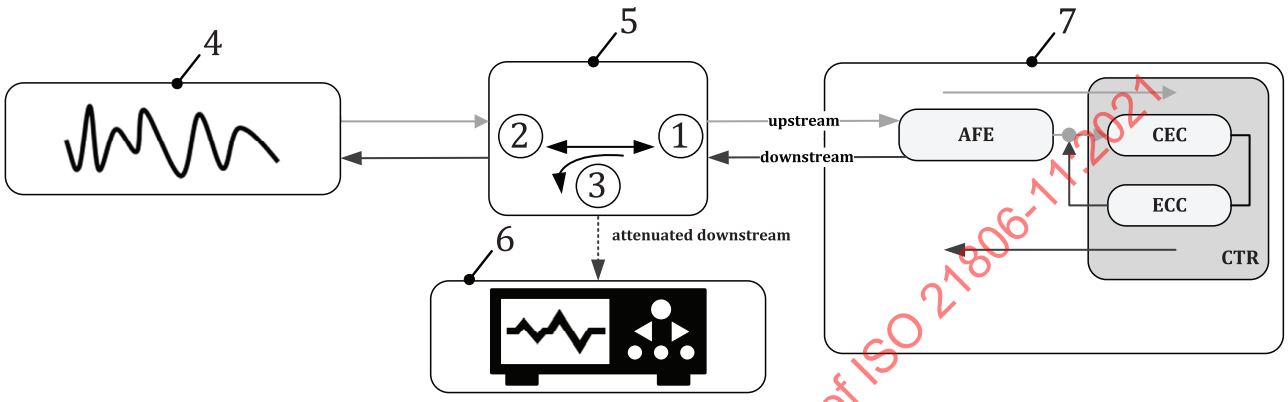


Key

1 pattern generator
2 ECport under test
3 oscilloscope

Figure 44 — SP2 jitter measurement set-up for duplex and standalone transceiver

For integrated transceivers the ECC input signal can be stimulated, using the bypass (see ISO 21806-10). As shown in Figure 45, the stimulus pattern is being transmitted upstream, through the directional coupler, through the CEC (including AFE), bypassed to the ECC input and then retransmitted by the ECC. The ECC output signal (again through the AFE) is transmitted downstream and a certain portion of the signal energy is transferred to the out-coupled path of the directional coupler. The ECC provides a reshaping of the output signal but no retiming. Therefore, the measured signal can be used for direct evaluation of transition times and steady state amplitude. Timing distortion, however, includes contribution from ECC and CEC.

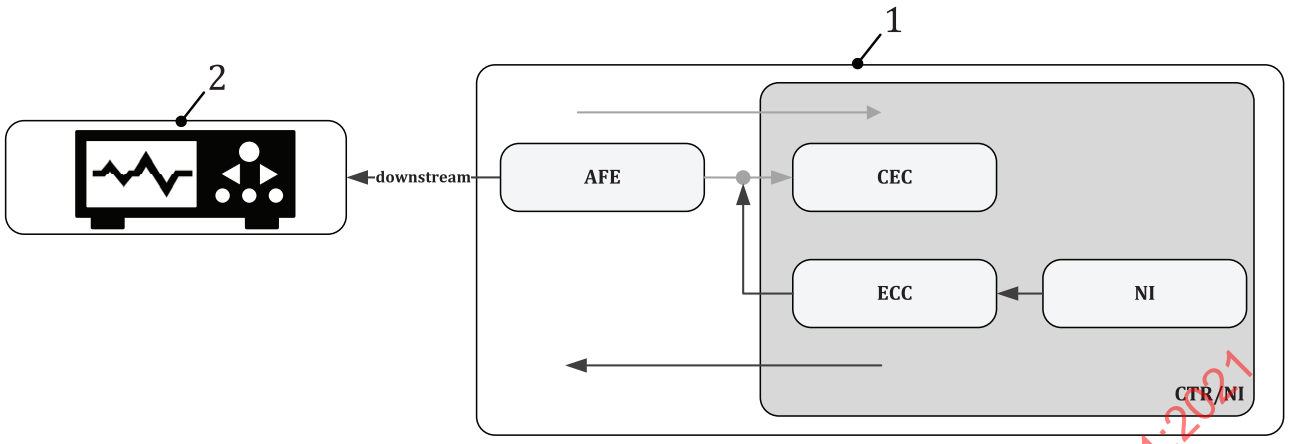


Key

1 terminal 1
2 terminal 2
3 terminal 3
4 SP3 stimulus
5 directional coupler
6 oscilloscope
7 ECport under test

Figure 45 — SP2 jitter measurement set-up for duplex and integrated transceiver 1

A reference of ECC performance shall be measured upfront and the result can be compensated for the CEC impact on the timing distortion. An example for such reference measurement is shown in Figure 46, it uses the pattern generated inside the MNC to get rid of impairments from CEC and the directional coupler.



Key

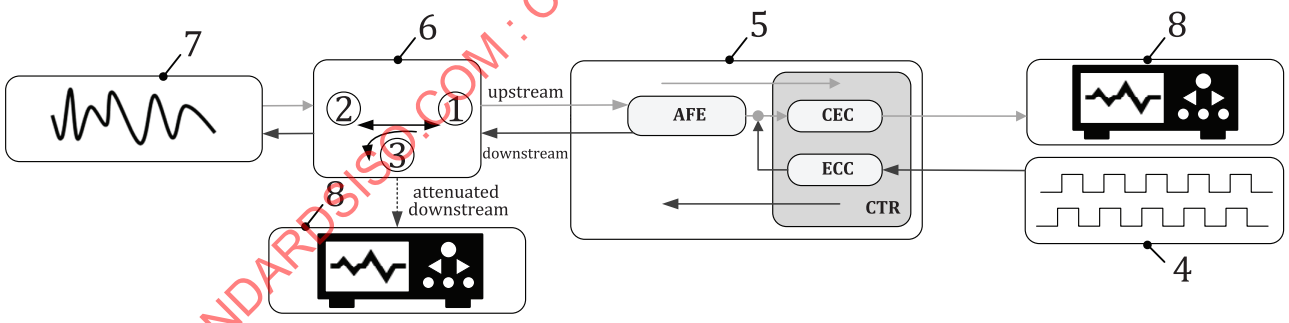
1 ECport under test
2 oscilloscope

Figure 46 — SP2 jitter measurement set-up for duplex and integrated transceiver, reference with data from MNC

10.4.4 SP4 jitter measurement (AJ and TJ) for duplex

As discussed in 8.9, there are several options to emulate influences on a transmission channel that degrade signal quality of an input signal at SP3. For duplex links this is mainly attenuation and crosstalk. Such impacts as well as the operating conditions of a coaxial receiver determine the signal quality at SP4.

Compared to simplex, the duplex test set-up is very similar. In addition, the back channel is implemented as shown in Figure 47 to test the CEC under full load. Optionally, a directional coupler can be implemented to visualize the back-channel signal, but this is not mandatory for this set-up.

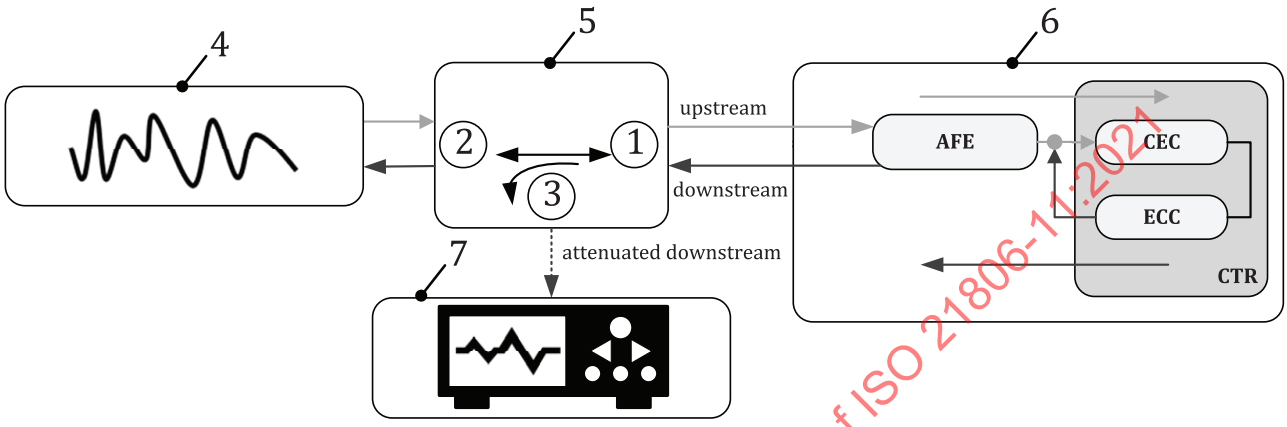


Key

1 terminal 1
2 terminal 2
3 terminal 3
4 pattern generator
5 CEport under test
6 directional coupler
7 SP3 stimulus
8 oscilloscope

Figure 47 — SP4 jitter measurement for duplex and standalone transceiver

For integrated transceivers the CEC output signal can be accessed, using the bypass (see ISO 21806-10). As shown in Figure 48, the stimulus pattern is being transmitted upstream, through the directional coupler, through the CEC (including AFE), bypassed to the ECC input and then retransmitted by the ECC. The ECC output signal (again through the AFE) is transmitted downstream and a certain portion of the signal energy is transferred to the out-coupled path of the directional coupler. The ECC provides a reshaping of the output signal but no retiming. Beside the CEC's response on various stimuli and test conditions, the resulting timing distortion includes contribution from ECC.

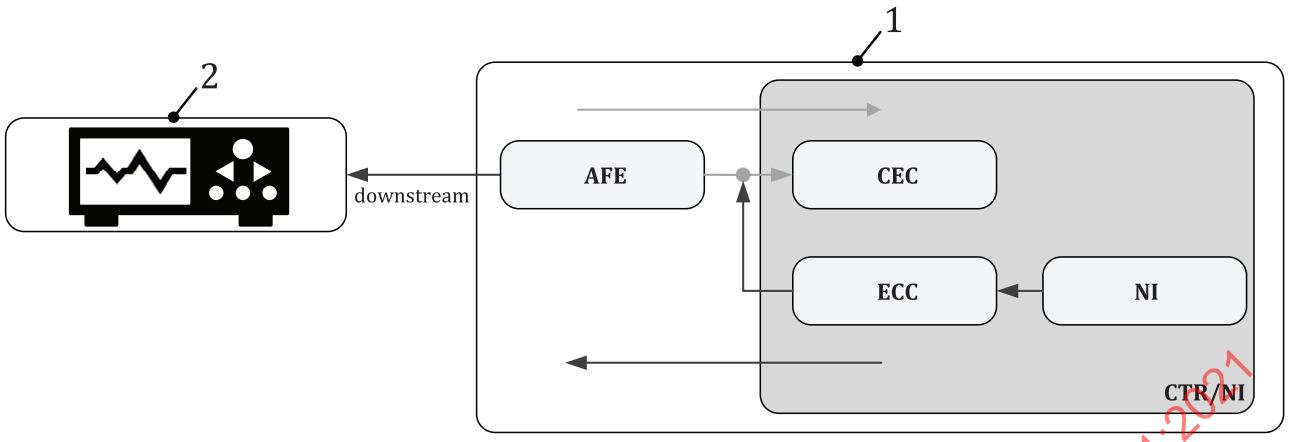


Key

1 terminal 1
2 terminal 2
3 terminal 3
4 SP3 stimulus
5 directional coupler
6 CEport under test
7 oscilloscope

Figure 48 — SP4 jitter measurement set-up for duplex and integrated transceiver

A reference of ECC performance shall be measured upfront. The timing distortion result can be compensated for the ECC impact. An example for such reference measurement is shown in Figure 49, it uses the pattern generated inside the MNC to eliminate impairments from CEC path.



Key

1 ECport under test

2 oscilloscope

Figure 49 — SP2 jitter measurement set-up for duplex and integrated transceiver, reference with data from MNC

11 Power-on and power-off

11.1 General

Clause 11 defines several possible test set-ups and sequences to exercise as many functional ECC and CEC requirements as possible and also provides guidelines for the interpretation of results.

All test sequences shall be performed for the minimum, typical, and maximum of the operating voltage according to operating conditions specified in 6.1.

All test sequences shall be performed for the minimum, typical, and maximum temperature specifications.

When testing MOST modules (ECC and CEC in one enclosure), crosstalk effects should be considered. When testing one MOST module, the other MOST modules shall be active.

Some of the parameters specified in ISO 21806-10:2021, Clause 10 can be measured (t_{STATF}, t_{LVDSV4}, etc.), other parameters (t_{ON2}, t_{OFF2}, t_{ON4}, etc.) determine relations between operation states and do not have distinct boundaries. For the parameters that cannot be measured, this clause specifies test sequences including a timeout, which represents the maximum and minimum time interval allowed for the respective parameter. The end of the interval is marked as action point in the signal charts (see Figure 51). It defines the time for a state validity evaluation.

For example, t_{ON2}(max.) time after the /RST signal transitions to logic 1, start evaluating the SP2 signal quality to check for conformance to the requirements for valid MOST data.

Measuring electrical parameters such as LVTTL or LVDS conformance is beyond the scope of this document and not discussed in detail herein, but some guidelines are given to facilitate proper parameter interpretation.

Testing of activity detection for ECC is described in 11.2, followed by descriptions for CEC in 11.3. Set-ups and test cases are described based on standalone transceivers, showing input stimuli and expected response. For a simplified presentation, all test cases are shown in simplex mode. The requirements for activity detection in duplex are identical to the simplex ones. As an additional stress condition, a CEC in duplex would be tested in presence of an actively driving ECC.

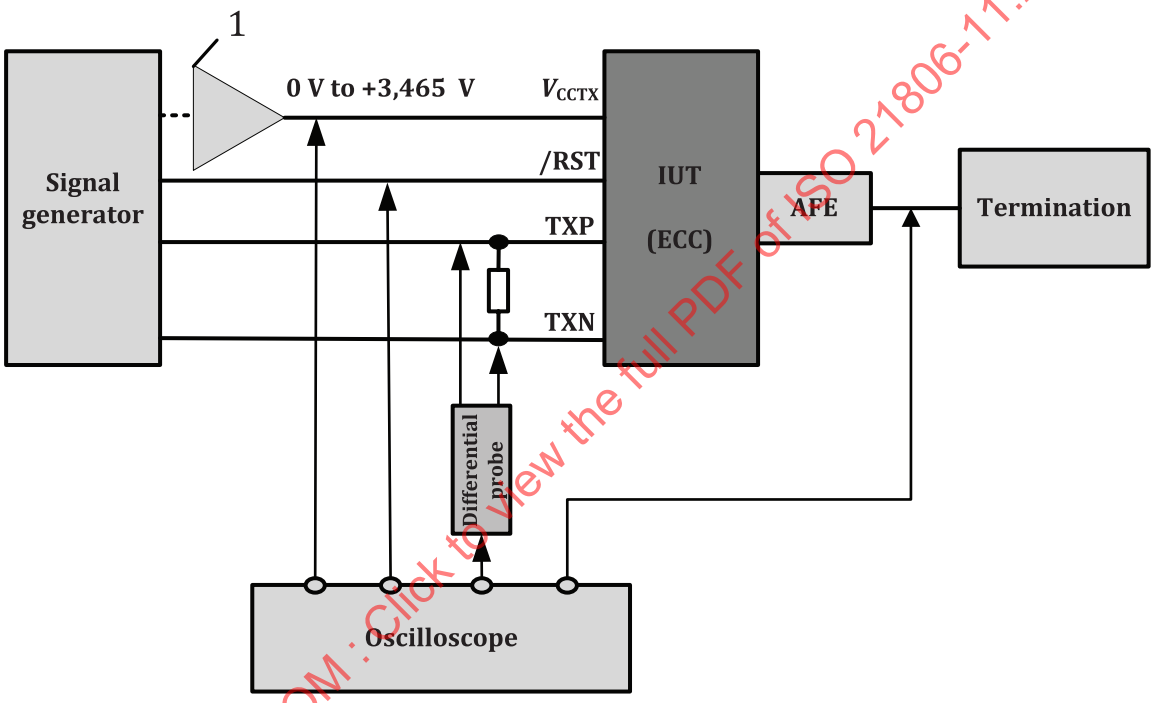
With integrated solutions as specified in ISO 21806-10, not all interfaces are accessible; therefore, a test case might not be applicable without modifications (e.g. SP1 signals are inside the IC). In such case, it is the responsibility of the ECC supplier to test the requested functionality in an appropriate way.

Testing of CEC's activity detection includes the full variety of scenarios being influenced by outer conditions, such as CEC power state requirements, SP2 signal performance of the preceding node, attenuation of coaxial interconnect, signal degradation due to RL (especially for duplex), etc.

11.2 Measuring ECC parameters

11.2.1 Measuring ECC parameters – Test set-up

Figure 50 shows an example of the test set-up for measurement of the ECC power-on and power-off.



Key

1 power amplifier/programmable power supply

Figure 50 — Set-up for measuring ECC power-on and power-off parameters

The main parts of the set-up are:

— the IUT is fitted according to the manufacturer's recommended set-up;

— the signal generator (i.e. pattern generator or arbitrary signal generator) is used to produce the stimuli (test patterns), produce a trigger signal, and control the ECC power supply;

— preferably the oscilloscope's internal 50 Ω termination can be used;

— the oscilloscope captures input and output signal data;

— the SP1 signal is a differential signal; an active differential probe should be used for measurement;

— the power amplifier/programmable power supply turns the ECC power on and off and provides the desired supply voltage.

11.2.2 Measuring ECC parameters – Signal charts

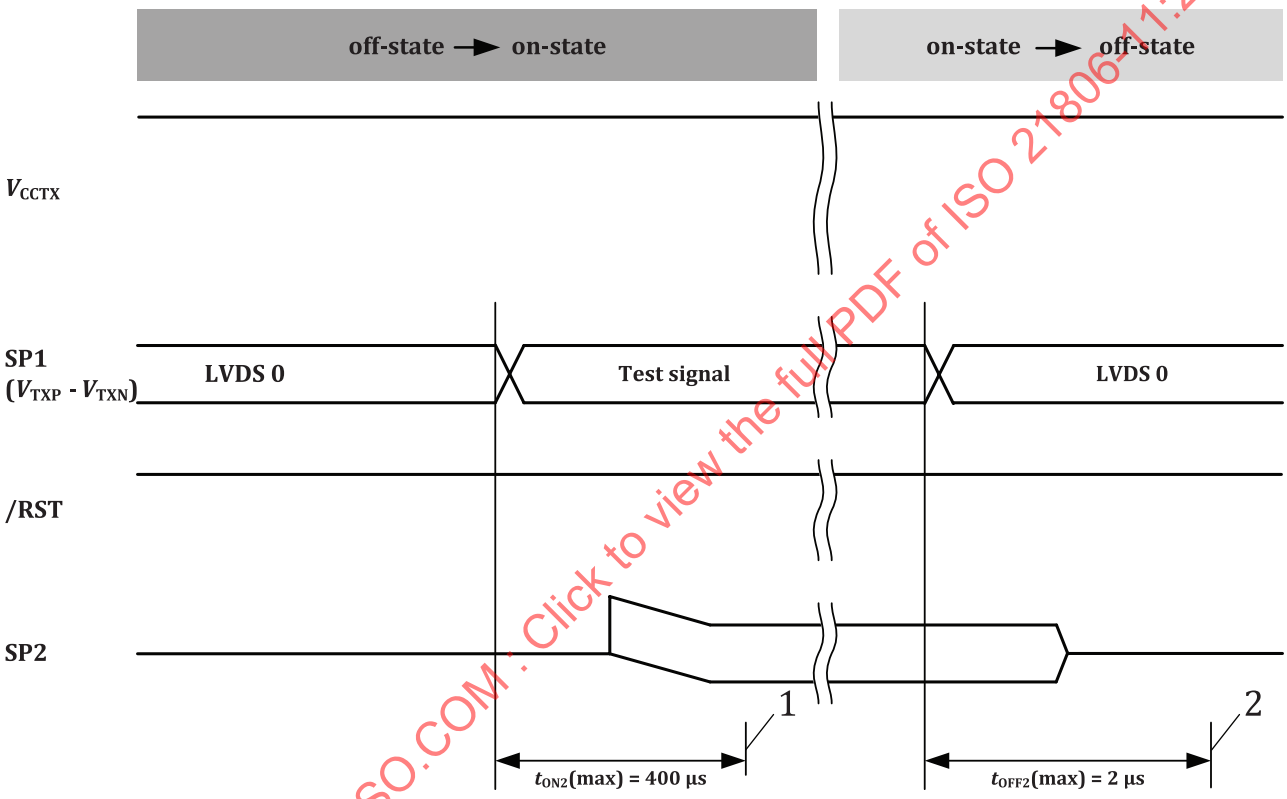
The signal charts represent the graphical view of test sequences. They show the location of the action points and provide the prerequisites for the corresponding tests for the ECC parameters.

The ECC parameter testing requires two different types of test sequences:

— in the first sequence, power-on and power-off behaviour is controlled by the signal content of SP1 while the /RST signal is logic 1 (Figure 51);

— in the second sequence, power-on and power-off behaviour is controlled by the /RST signal (Figure 52).

Figure 51 specifies the ECC signal chart No. 1 for measuring ECC parameters.



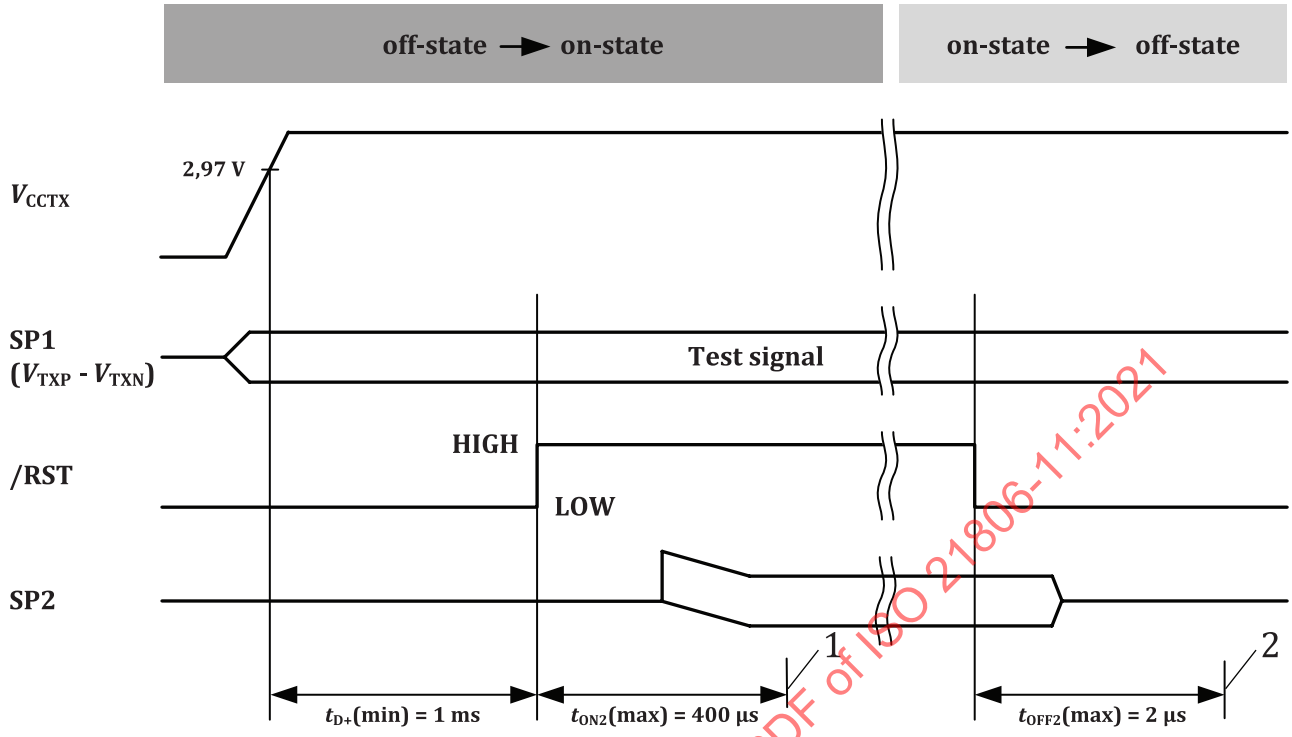
Key

1 marker action point 1

2 marker action point 2

Figure 51 — Measuring ECC parameters - ECC signal chart No. 1

Figure 52 defines the ECC signal chart No. 2 for measuring ECC parameters.



Key

1 marker action point 1

2 marker action point 2

Figure 52 — Measuring ECC parameters - ECC signal chart No. 2

11.2.3 Measuring ECC parameters – Test sequences

11.2.3.1 ECC test sequence #1 - off-state to on-state by SP1 signal

Table 14 specifies the ECC test sequence #1, which checks the transition detection mechanism of the ECC.

Table 14 — ECC test sequence #1

Item	Content
Signal chart	Figure 51
Initial state: inputs	V_{CCTX}: 0 V to 3,465 V /RST: logic 1 SP1 (V_{TXP} - V_{TXN}): LVDS 0
Initial state: output	SP2: off-state
Test signal: inputs	SP1 (V_{TXP} - V_{TXN}): 10 kHz square wave pattern LVDS compliant
Output/expected behaviour	ECC remains in off-state, supplied with an input signal and frequency within F_{OFF1} requirements.

An oscilloscope shall monitor the SP2 output before, during and after the test to ensure the off-state requirement is met.

11.2.3.2 ECC test sequence #2 – off-state to on-state by SP1 signal

Table 15 specifies the ECC test sequence #2, which checks the transition detection mechanism of the ECC. In this particular test the F_{ON1}(min.) conformance is checked.

Table 15 — ECC test sequence #2

Item	Content
Signal chart	Figure 51
Initial state: inputs	V_{CCTX}: 0 V to 3,465 V /RST: logic 1 SP1 (V_{TXP} - V_{TXN}): LVDS 0 0 Hz to 10 kHz square wave pattern LVDS compliant
Initial state: output	SP2: off-state
Test signal: inputs	SP1 (V_{TXP} - V_{TXN}): 12 MHz square wave pattern LVDS compliant
Output/expected behaviour	ECC transitions to on-state within time t_{ON2}(max.).

The oscilloscope shall check the maximum allowed transition time from off-state to on-state. ISO 21806-10:2021, Clause 10 mandates that the ECC is in on-state not later than t_{ON2}(max.) time after all on conditions are met. In this case, the start of t_{ON2} is triggered by the first rising edge of the test stimulus.

Since there is no measurable marker that indicates when the ECC enters the on-state, an indirect method is used: after the maximum allowed time [end of t_{ON2}(max.) – marked as action point 1 in the ECC signal Figure 51] a check of on-state requirements is started.

For this test, since the input is LVDS 0, only the SP2 signal amplitude is checked.

11.2.3.3 ECC test sequence #3 - on-state to off-state by SP1 signal

Table 16 specifies the ECC test sequence #3, which checks the transition detection mechanism of the ECC.

Table 16 — ECC test sequence #3

Item	Content
Signal chart	Figure 51
Initial state: inputs	V_{CCTX}: 0 V to 3,465 V /RST: logic 1 SP1 (V_{TXP} - V_{TXN}): 12 MHz LVDS compliant square wave
Initial state: output	SP2: on-state
Test signal: inputs	SP1 (V_{TXP} - V_{TXN}): LVDS 0 0 Hz to 10 kHz square wave pattern LVDS compliant
Output/expected behaviour	ECC transitions to off-state within time t_{OFF2} (max.).

The oscilloscope shall check the maximum allowed transition time from on-state to off-state. ISO 21806-10:2021, Clause 10 mandates that the ECC is in off-state not later than t_{OFF2}(max.) time after

one or more off conditions are met. In this case, the start of t_{OFF2} is triggered by the last falling edge of the initial state data pattern.

Since there is no measurable marker that indicates when the ECC enters the off-state, an indirect method is used: after the maximum allowed time [end of t_{OFF2}(max.) – marked as action point 2 in the ECC signal chart Figure 51], a check of off-state requirements is started.

The oscilloscope shall start monitoring the SP2 output after the time marked as action point 2 to ensure the off-state requirement is met.

To trigger the oscilloscope, the signal generator may produce a signal marker after t_{OFF2} (max.) time since switching the SP1 signal to LVDS 0 (or 10 kHz square wave form).

NOTE Long data set capture is preferred, since it is possible that the hold-off time that accompanies repetitive capture leads to missed events.

11.2.3.4 ECC test sequence #4 - off-state to on-state by SP1 signal

Table 17 specifies the ECC test sequence #4, which checks the transition detection mechanism of the ECC.

Table 17 — ECC test sequence #4

Item	Content
Signal chart	Figure 51
Initial state: inputs	V_{CCTX}: 0 V to 3,465 V /RST: logic 1 SP1 (V_{TXP} - V_{TXN}): LVDS 0 0 Hz to 10 kHz square wave pattern LVDS compliant
Initial state: output	SP2: off-state
Test signal: input	SP1 (V_{TXP} - V_{TXN}): LVDS compliant stress pattern with nominal ρ_{BR}
Output/expected behaviour	ECC transitions to on-state within time t_{ON2} (max.).

The oscilloscope shall check the maximum allowed transition time from off-state to on-state. ISO 21806-10:2021, Clause 10 mandates that the ECC is in on-state not later than t_{ON2} (max.) time after all on conditions are met. In this case, the start of t_{ON2} is triggered by the first rising edge of the test stimulus.

Since there is no measurable marker that indicates when the ECC enters the on-state, an indirect method is used: after the maximum allowed time [end of t_{ON2}(max.) – marked as action point 1 in the ECC signal chart Figure 51] a check of on-state requirements is started.

For this test, along with the output power of the SP2 interface, also the SP2 signal quality is checked. At action point 1, the oscilloscope shall start capturing the data sequence, which is used for evaluating the SP2 signal quality. To assist the capture of the SP2 data in on-state, the signal generator may assert the trigger signal to the oscilloscope t_{ON2} (max.) after activation of the test signal. Alternatively (if the signal generator does not have enough outputs), the oscilloscope is triggered by the SP1 signal with a delay of 100 µs.

11.2.3.5 ECC test sequence #5 - on-state to off-state by SP1 signal

Table 18 specifies the ECC test sequence #5, which checks the transition detection mechanism of the ECC.

Table 18 — ECC test sequence #5

Item	Content
Signal chart	Figure 51
Initial state: inputs	V_{CCTX}: 0 V to 3,465 V /RST: logic 1 SP1 (V_{TXP} - V_{TXN}): LVDS compliant stress pattern with nominal ρ_{BR}
Initial state: output	SP2: on-state
Test signal: inputs	SP1 (V_{TXP} - V_{TXN}): LVDS 0 0 Hz to 10 kHz square wave pattern LVDS compliant
Output/expected behaviour	ECC transitions to off-state within time t_{OFF2} (max.).

The oscilloscope shall check the maximum allowed transition time from on-state to off-state. ISO 21806-10:2021, Clause 10 mandates that the ECC is in off-state not later than t_{OFF2} (max.) time after one or more off conditions are met. In this case, the start of t_{OFF2} is triggered by the last falling edge of the initial state data pattern.

Since there is no measurable marker that indicates when the ECC enters the off-state, an indirect method is used: after the maximum allowed time [end of t_{OFF2} (max.) – marked as action point 2 in the ECC signal chart Figure 51] a check of off-state requirements is started.

The oscilloscope shall start monitoring the SP2 output after the time marked as action point 2 to ensure the off-state requirement is met.

To trigger the oscilloscope, the signal generator may produce a signal marker after t_{OFF2} (max.) time since switching the SP1 signal to LVDS 0 (or 10 kHz square wave form).

NOTE Long data set capture is preferred, since the hold-off time that accompanies repetitive capture can lead to missed events.

11.2.3.6 ECC test sequence #6 - off-state to on-state by /RST signal

Table 19 specifies the ECC test sequence #6, which checks the reset mechanism of the ECC and the minimal allowed time for the /RST signal to be set to logic 1 after the voltage provided by the power supply exceeds V_T.

Table 19 — ECC test sequence #6

Item	Content
Signal chart	Figure 52
Initial state: inputs	V_{CCTX}: 0 V to 3,465 V /RST: logic 0 SP1 (V_{TXP} - V_{TXN}): LVDS compliant stress pattern with nominal ρ_{BR}
Initial state: output	SP2: off-state
Test signal: inputs	/RST: logic 1
Output/expected behaviour	ECC transitions to on-state within time t_{ON2} (max.).

There are two aspects for treating this minimal allowed time.

The first is the power supply application aspect; the reset generator providing the signal shall be designed to ensure the /RST signal does not transition to logic 1 before t_{D+} (min.) time passes after the V_{CCTX} measured on the ECC power supply pins crosses V_T.

The second is the ECC parameter aspect; ISO 21806-10 mandates that when being supplied with an operating voltage within V_{ECCGR}, the internal circuitry of the ECC settles into stable operation with the ability to perform transition detection within a time defined by the minimum value of the parameter t_{D+}. By driving the /RST signal to logic 1 at the t_{D+} (min.) time it is checked if the ECC complies to that specification.

Since there is no measurable marker that indicates when the ECC enters the on-state, an indirect method is used for testing the t_{ON2}(max.) conformance: after the maximum allowed time [end of t_{ON2} (max.) – marked as action point 1 in the ECC signal chart Figure 52), a check of on-state requirements is started.

For this test, along with the output power of the SP2 interface, also the SP2 signal quality is checked. At action point 1, the oscilloscope shall start capturing the data sequence, which is used for evaluating the SP2 signal quality.

To assist the capture of the SP2 data in on-state, the signal generator may assert the trigger signal to the oscilloscope t_{ON2} (max.) after activation of the test signal. Alternatively (if the signal generator does not have enough outputs), the SP1 signal with a delay of 100 µs may be used to trigger the oscilloscope.

11.2.3.7 ECC test sequence #7 - on-state to off-state by /RST signal

Table 20 specifies the ECC test sequence #7, which checks the reset mechanism of the ECC.

Table 20 — ECC test sequence #7

Item	Content
Signal chart	Figure 52
Initial state: inputs	V_{CCTX}: 0 V to 3,465 V /RST: logic 1 SP1 (V_{TXP} - V_{TXN}): LVDS compliant stress pattern with nominal ρ_{BR}
Initial state: output	SP2: on-state
Test signal: inputs	/RST: logic 0
Output/expected behaviour	ECC transitions to off-state within time t_{OFF2} (max.) after the /RST signal is set to logic 0 and it stays in off-state as long as the /RST signal is logic 0.

Since there is no measurable marker that indicates when the ECC enters the off-state, an indirect method is used: after the maximum allowed time [end of t_{OFF2} (max.) – marked as action point 2 in the ECC signal chart Figure 52), a check of off-state requirements is started.

The oscilloscope shall start monitoring the SP2 output after the time marked as action point 2 to ensure the off-state requirement is met. A trigger signal from the signal generator is used to mark action point 2.

To trigger the oscilloscope, the signal generator may produce a signal marker t_{OFF2}(max.) time after switching the /RST signal to logic 0.

NOTE Long data set capture is preferred, since it is possible that the hold-off time that accompanies repetitive capture leads to missed events.

11.3 Measuring CEC parameters

11.3.1 Measuring CEC parameters – Test set-up

ISO 21806-10 specifies a set of functional requirements and performance parameters for the CEC. Figure 53 defines the set-up for measuring CEC power-on and power-off parameters.

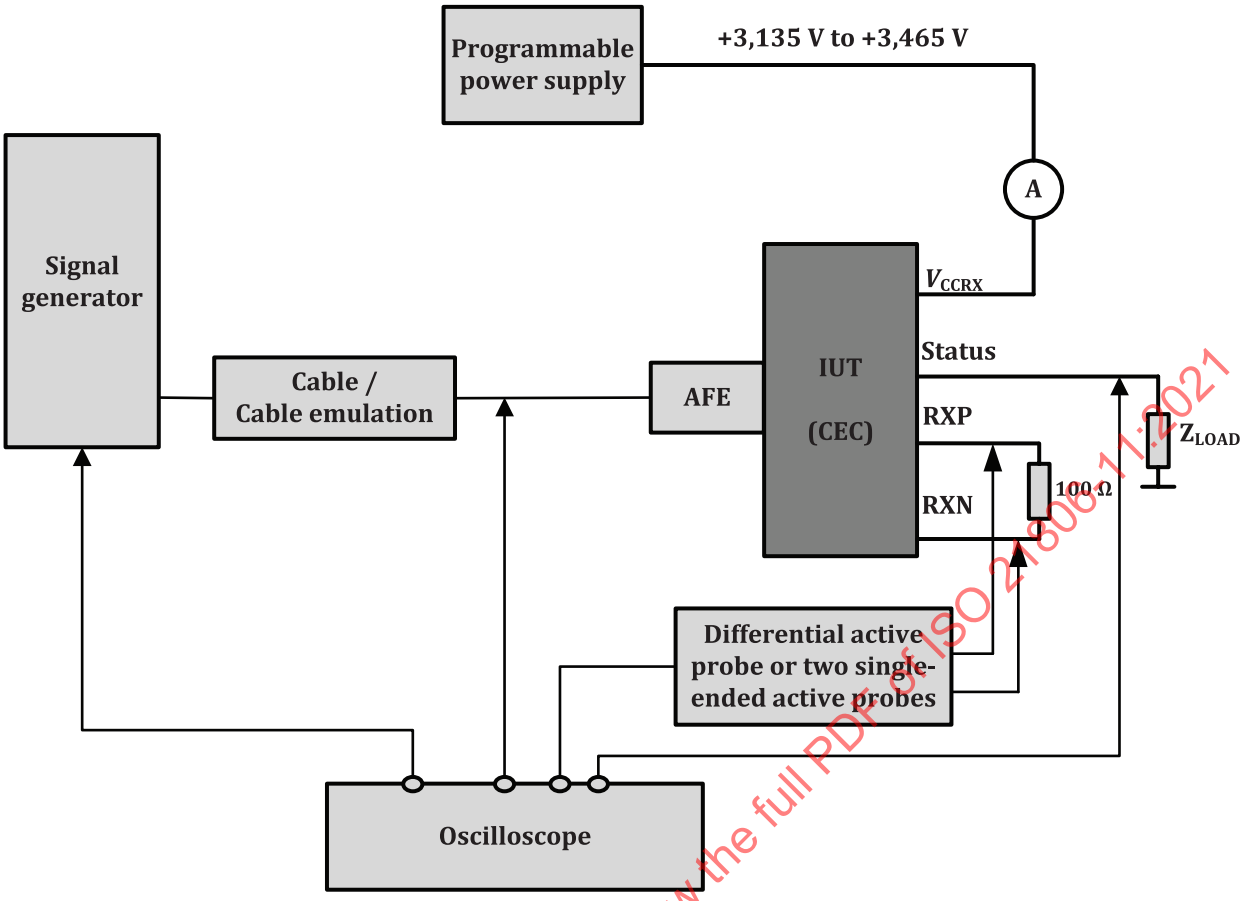


Figure 53 — Set-up for measuring CEC power-on and power-off parameters

The main parts of the set-up are:

— the IUT is fitted according to the manufacturer's recommended set-up and is powered constantly during the test(s);

— the cable or cable emulation emulates the degradation of data signals due to coaxial interconnects; the options to create a stimulus for SP3 interfaces as specified in 8.9 are also applicable here;

— the signal generator (i.e. pattern generator or arbitrary signal generator) is used to produce the test patterns and produce the trigger signal for the oscilloscope;

— the oscilloscope captures input and output signal data; the SP4 signal is a differential signal; an active differential probe should be used for measurement;

— the ampere meter measures the current consumption of the CEC under test (in off-state).

The signal generator shown in Figure 53 emulates the SP2 interface in a real network. Therefore, output signal amplitudes follow the specified values for SP2. In cases, where the cable emulation is already mathematically embedded in the signal generator's output patterns, amplitude settings follow SP2 amplitude values and the targeted cable degradation.

As a general rule, the signal amplitude at SP3 of the set-up emulates SP2 amplitudes and the targeted cable degradation. This is valid for the MOST150 cPHY stress pattern and for the square wave pattern used for testing CEC power state requirements. The signal generator and the cable or the cable emulation also shall provide an off-state as defined for the ECC (see ISO 21806-10).

NOTE CEC on-state and off-state depend on CEC power state requirements (F_{ON}, F_{OFF}) and signal amplitude limits, which are specified in ISO 21806-10.

Based on specification of SP2 steady state amplitudes, cable attenuation and RL in ISO 21806-10, signals with minimal amplitude for SP3 can be calculated. It is to be noted that the frequency dependent attenuation of the coaxial interconnect leads to different steady state amplitudes for pulses with different pulse width (2 UI, 3 UI, 4 UI, 5 UI, and 6 UI). Due to this effect, for every stimulus with specific (different) frequency content its corresponding minimal amplitude shall be calculated. In the context of this document this frequency (stimulus) dependent minimal amplitude is referred to as *minAMP_ON*.

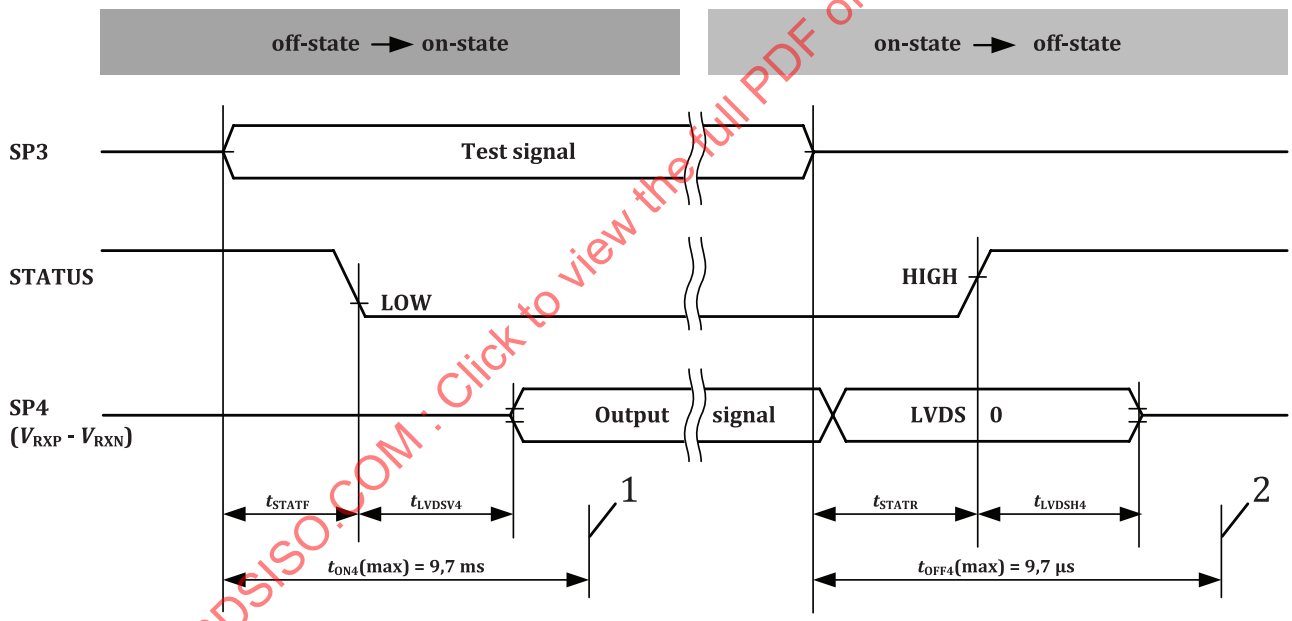
As a general requirement, a CEC shall be in on-state when CEC power state requirements are met and signal amplitudes equal or larger than the *minAMP_ON*.

With valid CEC power states requirements for on-state, there is no amplitude limit specified in ISO 21806-10 to enforce CEC off-state, nor can be derived. This is in the responsibility of the CEC-supplier. Such test cases, listed below, are marked "for information only". The corresponding amplitude condition is referred to as *maxAMP_OFF*.

11.3.2 Measuring CEC parameters – Signal charts

The signal chart represents the graphical view of test sequence. It defines the location of the action points and provides the prerequisites for the corresponding tests of the CEC parameters.

Figure 54 defines the measuring CEC parameters - CEC signal chart.



Key

1 marker action point 1

2 marker action point 2

Figure 54 — Measuring CEC parameters - CEC signal chart

11.3.3 Measuring CEC parameters – Test sequences

11.3.3.1 General

The test is performed according to the set-up described in 11.3.1.

11.3.3.2 CEC test sequence #1 – off-state to on-state

Table 21 specifies the CEC test sequence #1, which checks the transition detection and wake-up mechanism of the CEC.

Table 21 — CEC test sequence #1

Item	Content
Signal chart	Figure 54
Initial state: inputs	V_{CCRX}: 3,135 V to 3,465 V SP3: equivalent SP2 off-state
Initial state: output	STATUS: logic 1 SP4 (V_{RXP} - V_{RXN}): disabled
Test signal: inputs	SP3: continuous square wave between 0 Hz and 10 kHz
Output/expected behaviour	The CEC stays in off-state with STATUS logic 1 and SP4 outputs disabled. With input stimulus present, the CEC's current consumption may exceed $I_{CCSLEEP}$(max.).

The minimum and maximum values of the signal amplitude shall be tested. Test signals with multiple test signal levels should be used.

11.3.3.3 CEC test sequence #2 – off-state to on-state

Table 22 specifies the CEC test sequence #2, which checks the transition detection and wake-up mechanism of the CEC.

Table 22 — CEC test sequence #2

Item	Content
Signal chart	Figure 54
Initial state: inputs	V_{CCRX}: 3,135 V to 3,465 V SP3: equivalent SP2 off-state
Initial state: output	STATUS: logic 1 SP4 (V_{RXP} - V_{RXN}): disabled
Test signal: inputs	SP3: continuous 12 MHz square wave signal amplitude < *maxAMP_OFF*
Output/expected behaviour	The CEC stays in off-state with STATUS logic 1 and SP4 outputs disabled. With input stimulus present, the CEC's current consumption may exceed $I_{CCSLEEP}$(max.).

11.3.3.4 CEC test sequence #3 – off-state to on-state

Table 23 specifies the CEC test sequence #3, which checks the transition detection and wake-up mechanism of the CEC.

Table 23 — CEC test sequence #3

Item	Content
Signal chart	Figure 54
Initial state: inputs	V_{CCRX}: 3,135 V to 3,465 V SP3: equivalent SP2 off-state
Initial state: output	STATUS: logic 1 SP4 (V_{RXP} - V_{RXN}): disabled
Test signal: inputs	SP3: 12 MHz square wave burst with duration ≤ t_{STATF}(min.) amplitude > *minAMP_OFF*

Table 23 *(continued)*

Item	Content
Output/expected behaviour	The CEC stays in off-state with STATUS logic 1 and SP4 outputs disabled. With input stimulus present, the CEC's current consumption may exceed $I_{CCSLEEP}$(max.).

The minimum and maximum values of the signal amplitude shall be tested. Test signals with multiple test signal levels should be used.

11.3.3.5 CEC test sequence #4 – off-state to on-state

Table 24 specifies the CEC test sequence #4, which checks the transition detection and wake-up mechanism of the CEC.

Table 24 — CEC test sequence #4

Item	Content
Signal chart	Figure 54
Initial state: inputs	V_{CCRX}: 3,135 V to 3,465 V SP3: equivalent SP2 off-state
Initial state: output	STATUS: logic 1 SP4 (V_{RXP} - V_{RXN}): disabled
Test signal: inputs	SP3: 12 MHz square wave burst with duration > t_{STATF}(min.) amplitude > *minAMP_OFF*
Output/expected behaviour	The CEC transitions to on-state within time t_{ON4}(max.) with STATUS logic 0 within t_{STATF}(min.) to t_{STATF}(max.), and valid LVDS levels within t_{LVDSV4}(max.).

The input signal represents no valid MOST data. Therefore, only the STATUS signal timing and SP4 LVDS conformance shall be checked.

The minimum and maximum values of the signal amplitude shall be tested. Test signals with multiple test signal levels should be used.

11.3.3.6 CEC test sequence #5 – on-state to off-state

Table 25 specifies the CEC test sequence #5, which checks the transition detection and shutdown mechanism of the CEC.

Table 25 — CEC test sequence #5

Item	Content
Signal chart	Figure 54
Initial state: inputs	V_{CCRX}: 3,135 V to 3,465 V SP3: continuous 12 MHz square wave amplitude > *minAMP_OFF*
Initial state: output	STATUS: logic 0 SP4 (V_{RXP} - V_{RXN}): LVDS compliant signal
Test signal: inputs	SP3: signal amplitude < *maxAMP_OFF*
Output/expected behaviour	The CEC transitions to off-state with STATUS logic 1 within t_{STATR}(max.) and SP4 outputs disabled within t_{OFF4}(max.), but not earlier than t_{LVDSH4}(min.) after STATUS transitions to logic 1. After t_{OFF4}(max.), the CEC's current consumption is below $I_{CCSLEEP}$(max.).

To trigger the start of the electrical current measurement, the signal generator may assert the trigger signal to the ampere meter t_{OFF4}(max.) after application of the test signal to allow the ampere meter to perform current consumption measurement (used in t_{OFF4} requirement evaluation).

The minimum and maximum values of the signal amplitude shall be tested. Test signals with multiple test signal levels should be used.

11.3.3.7 CEC test sequence #6 – off-state to on-state

Table 26 specifies the CEC test sequence #6, which checks the transition detection and wake-up mechanism of the CEC.

Table 26 — CEC test sequence #6

Item	Content
Signal chart	Figure 54
Initial state: inputs	V_{CCRX}: 3,135 V to 3,465 V SP3: MOST150 cPHY stress pattern with nominal ρ_{BR} signal amplitude < *maxAMP_OFF*
Initial state: output	STATUS: logic 1 SP4 (V_{RXP} - V_{RXN}): disabled
Test signal: inputs	SP3: amplitude > *minAMP_OFF*
Output/expected behaviour	The CEC transitions to on-state within time t_{ON4}(max.) with STATUS logic 0 within t_{STATF}(min.) to t_{STATF}(max.), and valid LVDS levels within t_{LVDSV4}(max.)

Since there is no measurable marker that indicates when the CEC enters the on-state, an indirect method is used for the t_{ON4}(max.) parameter evaluation: after the maximum allowed time [end of t_{ON4}(max.) – marked as action point 1 in the signal chart Figure 54] a check of on-state requirements is started.

For this test, along with checking for STATUS logic 0, the SP4 signal quality is evaluated. At action point 1, the oscilloscope shall start capturing the data sequence, which is used for evaluating the SP4 signal quality. To assist the capture of the SP4 data, the signal generator may assert the trigger signal to the oscilloscope t_{ON4}(max.) after activation of the test signal. Alternatively (if the signal generator does not have enough outputs), the oscilloscope may be triggered by the SP1 signal with a delay of 10 ms.

The minimum and maximum values of the signal amplitude shall be tested. Test signals with multiple test signal levels should be used.

11.3.3.8 CEC test sequence #7 – on-state to off-state

Table 27 specifies the CEC test sequence #7, which checks the transition detection and shutdown mechanism of the CEC.

Table 27 — CEC test sequence #7

Item	Content
Signal charts	Figure 54
Initial state: inputs	V_{CCRX}: 3,135 V to 3,465 V SP3: MOST150 cPHY stress pattern with nominal ρ_{BR} signal amplitude > *minAMP_OFF*
Initial state: output	STATUS: logic 0 SP4 (V_{RXP} - V_{RXN}): LVDS compliant valid MOST data
Test signal: inputs	SP3: signal amplitude < *maxAMP_OFF*

Table 27 *(continued)*

Item	Content
Output/expected behaviour	The CEC transitions to off-state with STATUS = logic 1 within t_{STATR}(max.) and SP4 outputs disabled within t_{OFF4}(max.), but not earlier than t_{LVDSH4}(min.) after STATUS transitions to logic 1. After t_{OFF4}(max.), the CEC's current consumption is below $I_{CCSLEEP}$(max.).

To trigger the start of the electrical current measurement, the signal generator may assert the trigger signal to the ampere meter t_{OFF4}(max.) after application of the test signal to allow the ampere meter to perform current consumption measurement (used in t_{OFF4} requirement evaluation).

The minimum and maximum values of the signal amplitude shall be tested. Test signals with multiple test signal levels should be used.

12 Detecting bit rate (frequency reference)

The bit rate is detected as follows.

— Data-pulses range from 2 UI to 6 UI yielding five different pulse widths (2 UI, 3 UI, 4 UI, 5 UI, and 6 UI). A clock at UI rate represents a cycle time of 1 UI, which is twice the bit rate (i.e. for a ρ_{Fs} of 48 kHz, the bit rate is 147,45 Mbit/s and the UI clock is 294,91 MHz).

— A method of extracting the UI clock out of a waveform is a mandatory function to be provided with the oscilloscope. In a first step, the recovered UI clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency. The approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only. Then the bit rate is half the UI rate.

— The bit rate can be measured with the MOST150 cPHY stress pattern or any other valid data pattern. Set-up of the oscilloscope shall follow the general requirements (see 6.2) using acquisition length of 10 megasample and a sampling rate of 10 gigasample/s.

13 System performance

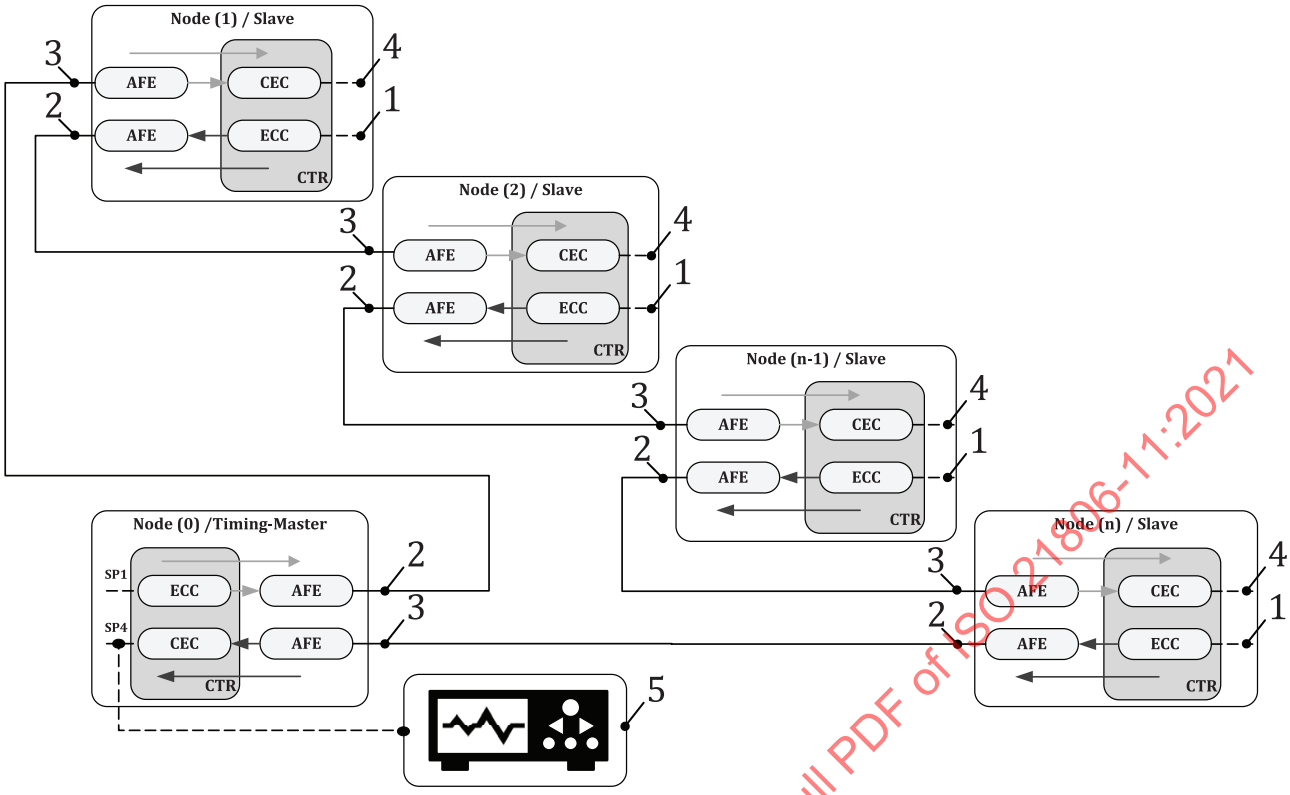
13.1 General

The system-level specifications apply to an entire MOST network.

13.2 SP4 receiver tolerance

Unlike the link-level tests, which use a pattern generator as the signal source, the system-level tests use live data from a MOST150 network. Using the eye diagram methodologies described in Clause 9, a measurement is taken at SP4 of the TimingMaster node. By taking the measurement in this way, one can quantify the total jitter accumulation in the network. This measurement is applicable for every node in the network at SP4.

Figure 55 shows the SP4 receiver tolerance set-up.



Key

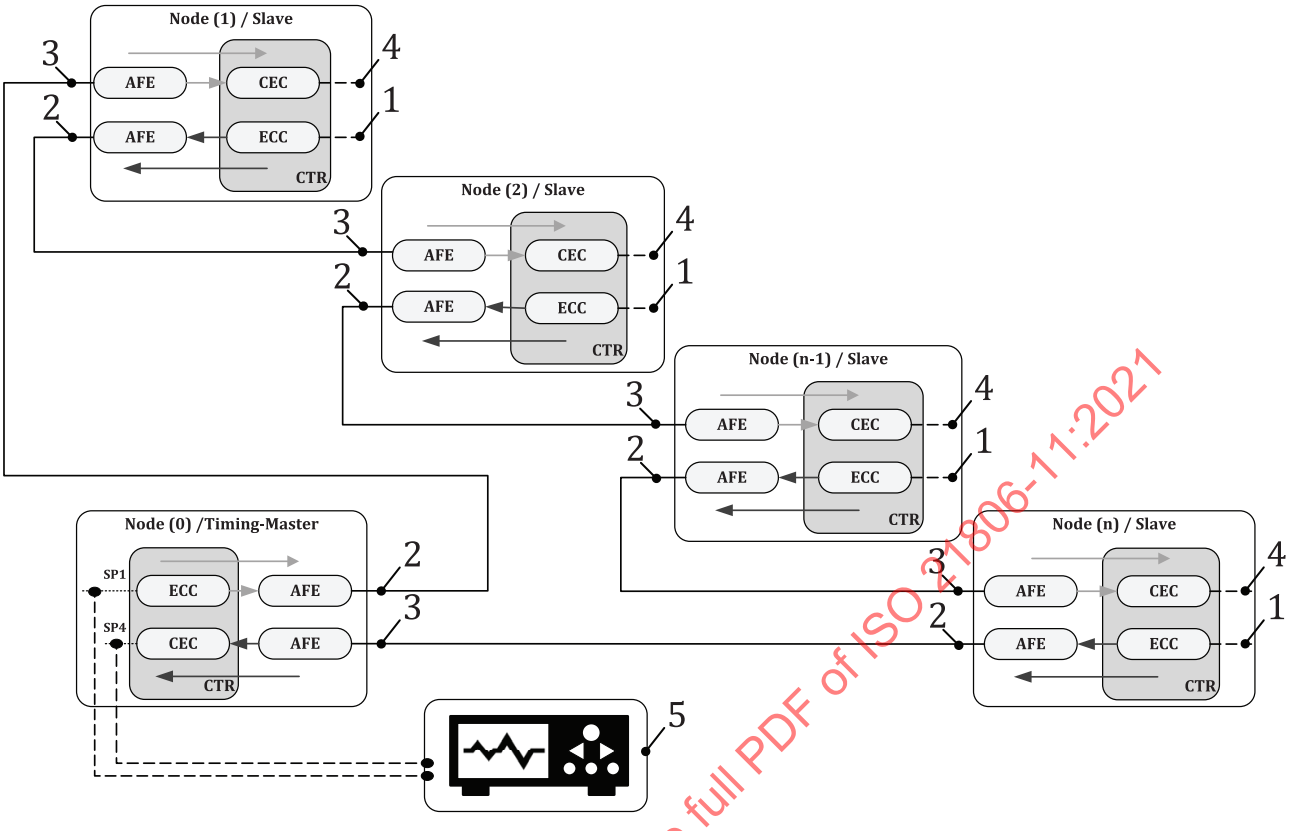
1 SP1
2 SP2
3 SP3
4 SP4
5 oscilloscope

Figure 55 — SP4 receiver tolerance set-up

13.3 TimingMaster delay tolerance

TimingMaster delay tolerance is a measure of end-to-end delay and phase variation between SP1 and SP4 of the MOST device that contains the TimingMaster. To ensure proper network operation, the total network delay shall not exceed the specified maximum (see ISO 21806-10:2021, 11.2).

Following the set-up diagram shown in Figure 56, the total delay can be measured with an oscilloscope.



Key

1 SP1
2 SP2
3 SP3
4 SP4
5 oscilloscope

Figure 56 — TimingMaster delay tolerance set-up

Table 28 specifies the procedure used to measure the total delay. The oscilloscope used shall be able to trigger on a specified period and shall have software functions for tracking periods. Two differential probes are needed.

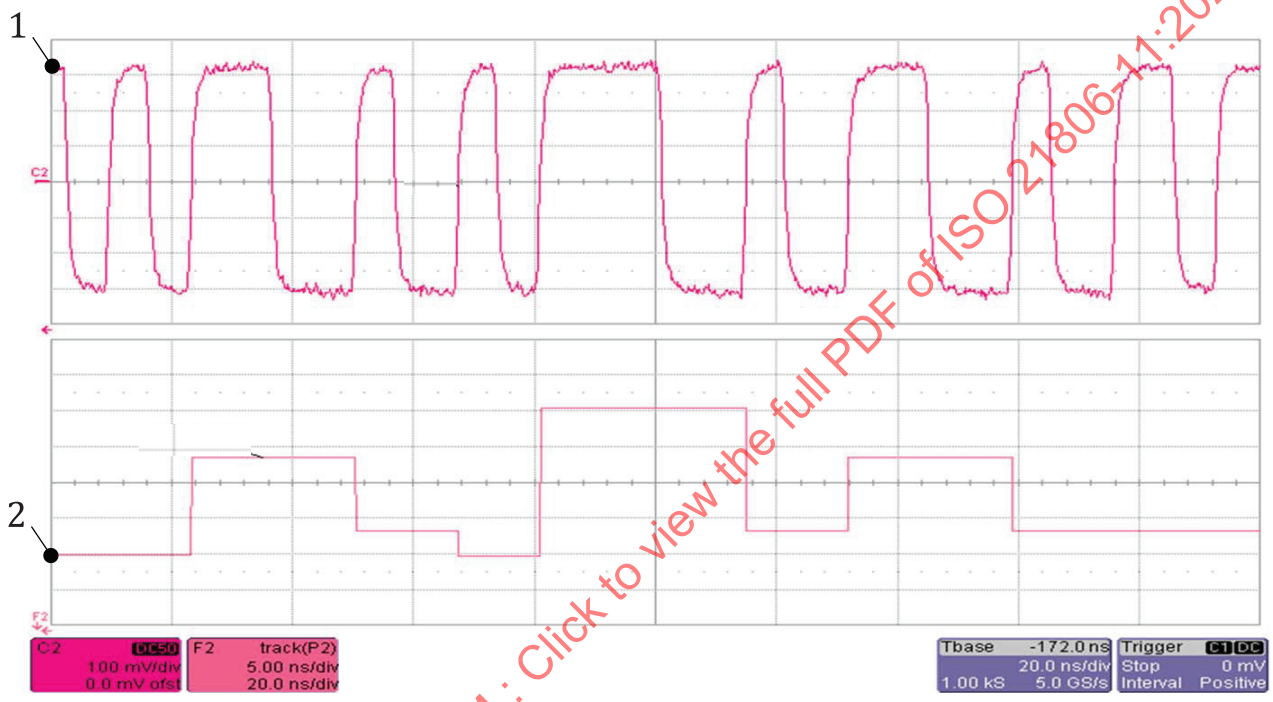
Table 28 — TimingMaster delay measurement procedure

Action	Description
Acquire a waveform	For this measurement, the sampling memory of the oscilloscope should be adjusted to capture at least one frame of data. One differential probe is connected to SP1 of the TimingMaster node. A second differential probe is connected to SP4 of the TimingMaster node. The vertical scale is adjusted to achieve sufficient vertical resolution on both channels. The trigger settings are adjusted to trigger on the interval of rising edges (period) on SP1. The interval should be set to 10 UI ± 0,5 UI. The trigger mode should be normal. A sequence of the data stream ("waveform") is sampled into the oscilloscope's memory.
Measure the period	The MOST150 data stream contains a period of 10 UI at the start of each frame. This long period can be used as a marker to measure the delay between any two points in the network. Configure the oscilloscope to measure the period of both SP1 and SP4.

Table 28 *(continued)*

Action	Description
Track the period	Configure the oscilloscope to display a “track” waveform for both SP1 and SP4 period measurements. This should result in two waveforms (see Figure 57 and Figure 58) with time on the y-axis where the line indicates the length of the current period.
Measure the delay	Configure the oscilloscope display to show only the SP1 and SP4 period tracks. Turn on infinite persistence and adjust the display to show the 10 UI segment for both SP1 and SP4. Using the cursor, measure the total time between the trigger point and the rightmost edge of the SP4 10 UI period. This is the TimingMaster delay.

Figure 57 shows an example of tracking the SP4 period.



Key

1 acquired data signal at SP4

2 measured period at SP4

Figure 57 — Example of tracking the SP4 period

Figure 58 shows how the TimingMaster delay is measured.

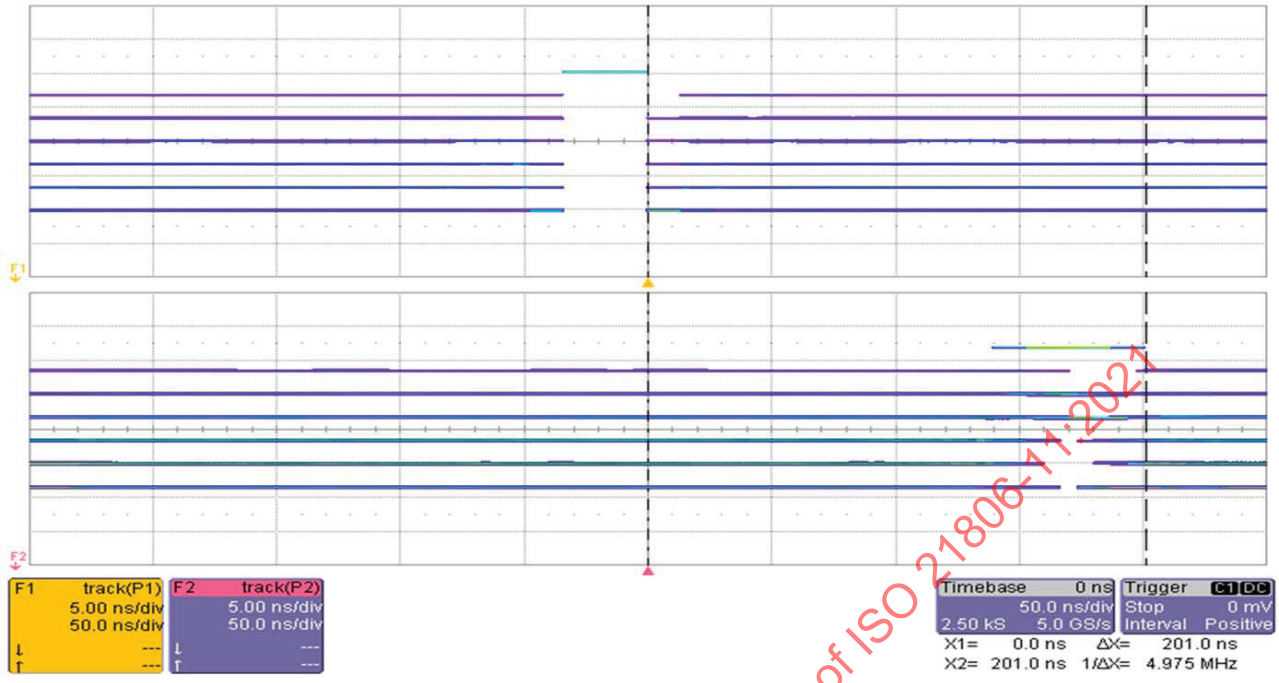


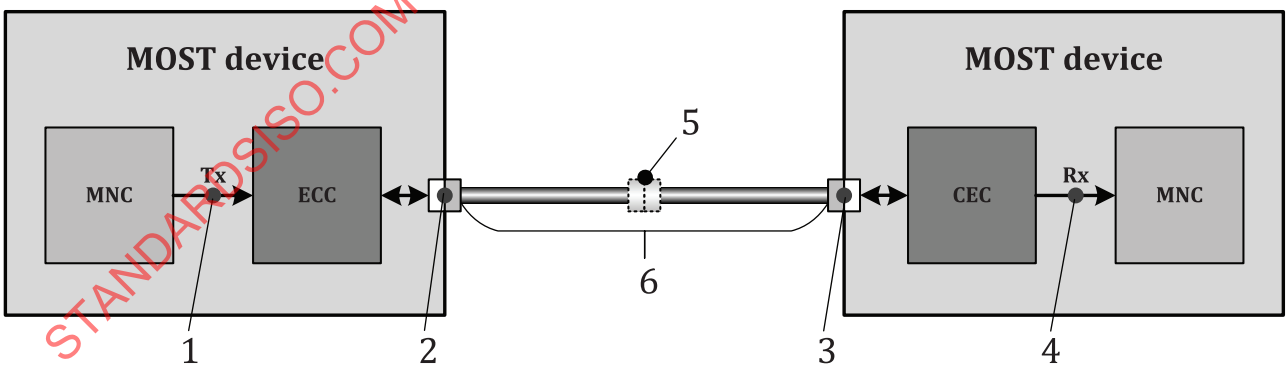
Figure 58 — TimingMaster delay

14 Conformance tests of 150-Mbit/s coaxial physical layer

14.1 Location of interfaces

SP1 describes input parameters for the ECC. It also describes the output parameters of an MNC, including data path between MNC and ECC. SP2 describes the coaxial output signal.

Figure 59 shows the SP locations for simplex interconnect.

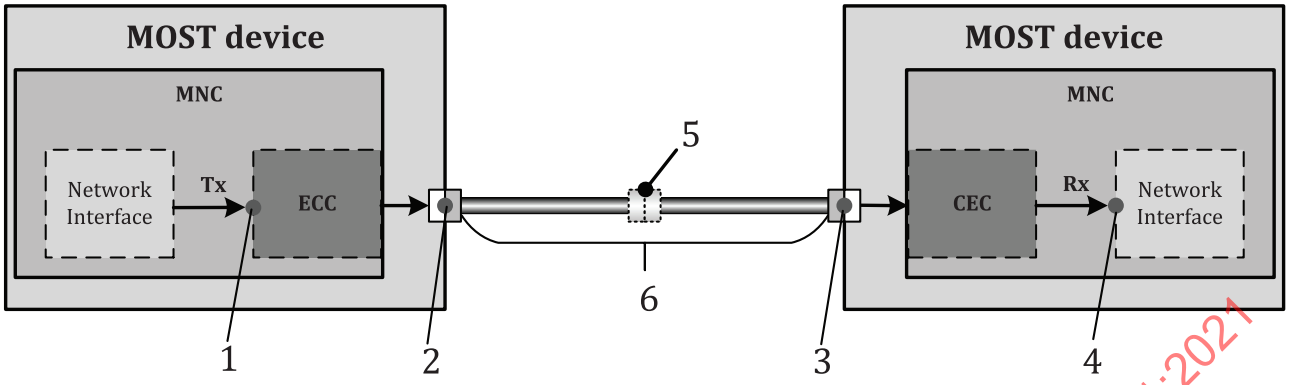


Key

1 SP1
2 SP2
3 SP3
4 SP4
5 in-line connectors (optional)
6 50 Ω coaxial interconnect (including connectors)

Figure 59 — SP locations for simplex interconnect

Figure 60 shows the SP locations for simplex interconnect with integrated coaxial transceivers.

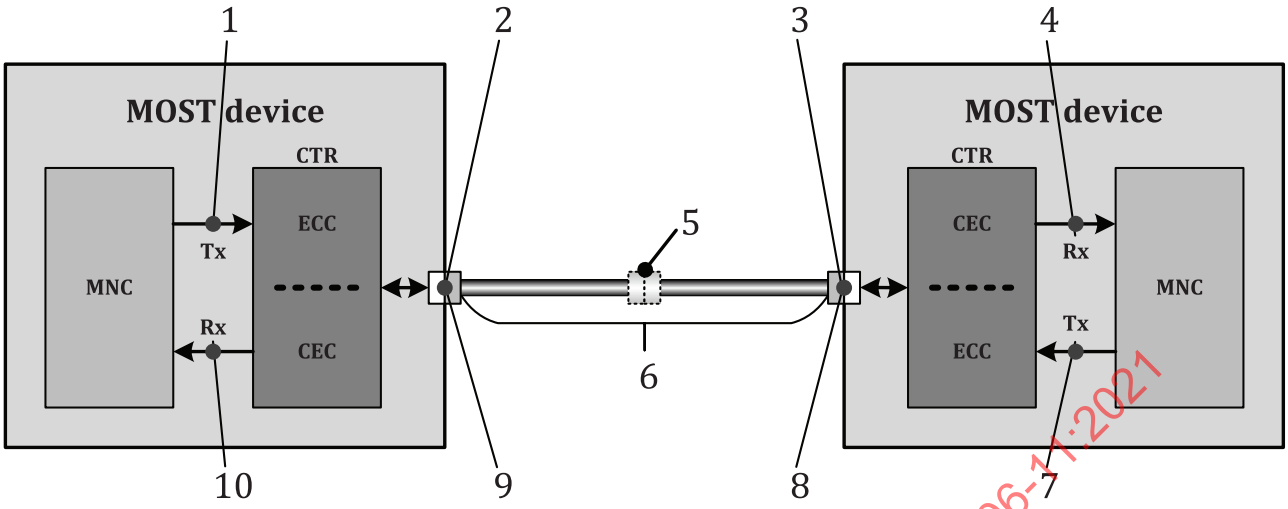


Key

1 SP1
2 SP2
3 SP3
4 SP4
5 in-line connectors (optional)
6 50 Ω coaxial interconnect (including connectors)

Figure 60 — SP locations for simplex interconnect with integrated coaxial transceivers

Figure 61 shows the SP locations for duplex interconnect.

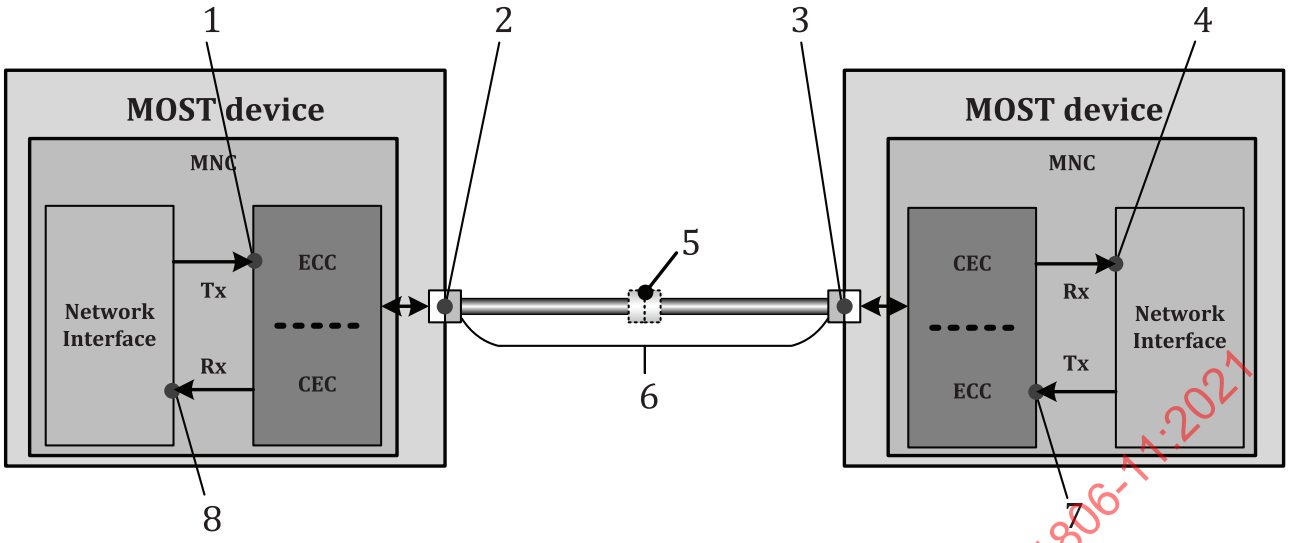


Key

1	SP1
2	SP2
3	SP3
4	SP4
5	in-line connectors (optional)
6	50 Ω coaxial interconnect (including connectors)
7	SP1*
8	SP2*
9	SP3*
10	SP4*

Figure 61 — SP locations for duplex interconnect

Figure 62 shows the SP locations for duplex interconnect with integrated coaxial transceivers.



Key

1 SP1
2 SP2
3 SP3
4 SP4
5 in-line connectors (optional)
6 50 Ω coaxial interconnect (including connectors)
7 SP1*
8 SP4*

Figure 62 — SP locations for duplex interconnect with integrated coaxial transceivers

SP3 describes the coaxial input interface for the CEC. Signal characteristics at SP3 consider worst-case coaxial signal according to the SP2 definition plus deterioration due to the transport media.

SP4 link quality describes the output parameters for CECs including termination. SP4 receiver tolerance describes the input tolerance for MNCs and is relevant for system evaluation.

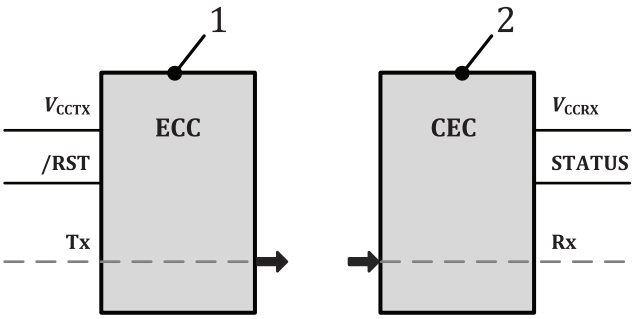
Signals that fulfil the SP4 parameters can be recovered by the MNC; signals outside the ranges might cause bit errors. On Tx of the MNC (node n + 1) a recovered signal is available according to SP1 requirements and timing distortion (except transferred jitter) is eliminated.

14.2 Control signals

In addition to power supply terminals and data pins, an ECC provides an /RST input. The ECC provides activity detection in order to enable/disable MOST output. Activity depends on the V_{CC} state, data content of SP1, and reset state.

The CEC also provides activity detection, depending on the characteristics of the input signal (power level, signal content). on-state/off-state is signalled by the STATUS pin. There exists both a standalone and an integrated version of CEC/ECC.

Figure 63 shows the control signals for power-on and power-off behaviour (standalone).



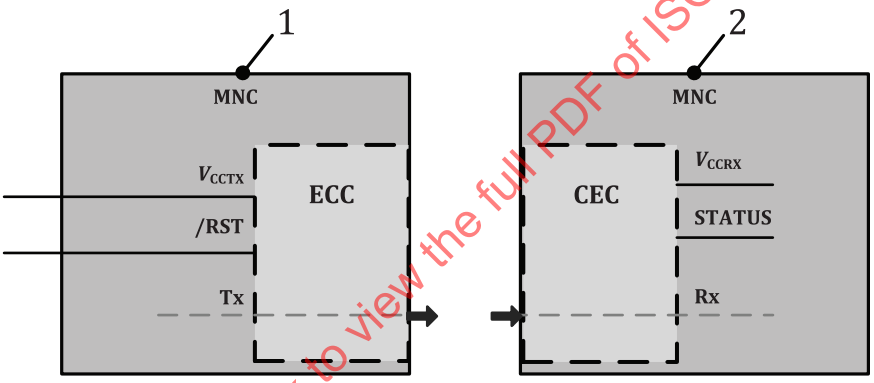
Key

1 ECC power-on and power-off parameters

2 CEC power-on and power-off parameters

Figure 63 — Control signals for power-on and power-off behaviour (standalone)

Figure 64 shows the control signals for power-on and power-off behaviour (integrated).



Key

1 ECC power-on and power-off parameters

2 CEC power-on and power-off parameters

Figure 64 — Control signals for power-on and power-off behaviour (integrated)

14.3 Limited access to specification points

On MOST device level, measurement has no access to SP1 and SP4. Therefore, conformance verification on MOST component and MOST module level is required. This is a precondition for simplification of the conformance verification of MOST devices, using the limited (access) conformance procedure.

Variation on input parameters can only be applied at SP3 (coaxial signal input of the MOST device). Parameters can only be measured at SP2. The power supply of the MNC, ECC and CEC is fixed by the design of the MOST device and cannot be varied. Considering these circumstances, the limited physical layer conformance specifies a simplified test procedure that uses only the accessible interfaces of a MOST device, SP2 and SP3 (see Clause 15).

14.4 Parameter overview

Table 29 specifies the conformance procedures for the parameters of ISO 21806-10 that are relevant for physical layer conformance. For each parameter, it indicates how conformance can be achieved, depending on the type: MOST component (ECC/CEC), MOST module, or MOST device.

NOTE Developers of MOST components or MOST modules ensure that their products fulfil the specification under minimum/maximum conditions of their input parameters, considering environmental conditions and lifetime. The verification of these parameters is done using the procedure of the product characterization.

Table 29 — Conformance procedures for all parameters of specification points

SP	Parameter	Conformance procedure
SP2	Output V_{SS} steady-state amplitude	M[a] (T, U)
	Transition time (rise and fall)	M[a] (T, U)
	Alignment jitter acc. to eye mask	M[a] (T, U)
	Transferred jitter (RMS)	M[a] (T, U)
	RL of ECU interface	M[a] (T_{Typ}) (only duplex)
SP3	Limited physical layer test of data consistency	M[a] (T, U)
	RL of ECU interface	M[a] (T_{Typ}) (simplex, duplex)
[a] M = measure (T = temperature range, T_{Typ} typical temperature, U = voltage range).		

The conformance verification of development tools is described in Annex A. The status of Annex A is informative.

15 Limited physical layer conformance

15.1 Overview

Limited physical layer conformance refers to MOST devices (see 14.3).

Generally, conformance testing requires access to all specification points. In addition, various test signals are applied to a particular interface in order to check worst-case performance of components and modules that are connected to that interface. The physical layer conformance test considers all environment conditions (e.g., specified operating temperature, power supply variations).

An overview of the parameters to be tested and verified is shown in Table 29.

Figure 65 specifies the test set-up for limited physical layer verification comprising the following equipment:

— MOST150 physical layer stress test tool (PHYSTT)[4];

— MOST150 cPHY tester cable model (MTCM)[8];

  — attenuator;

  — cable representation;

  — directional coupler;

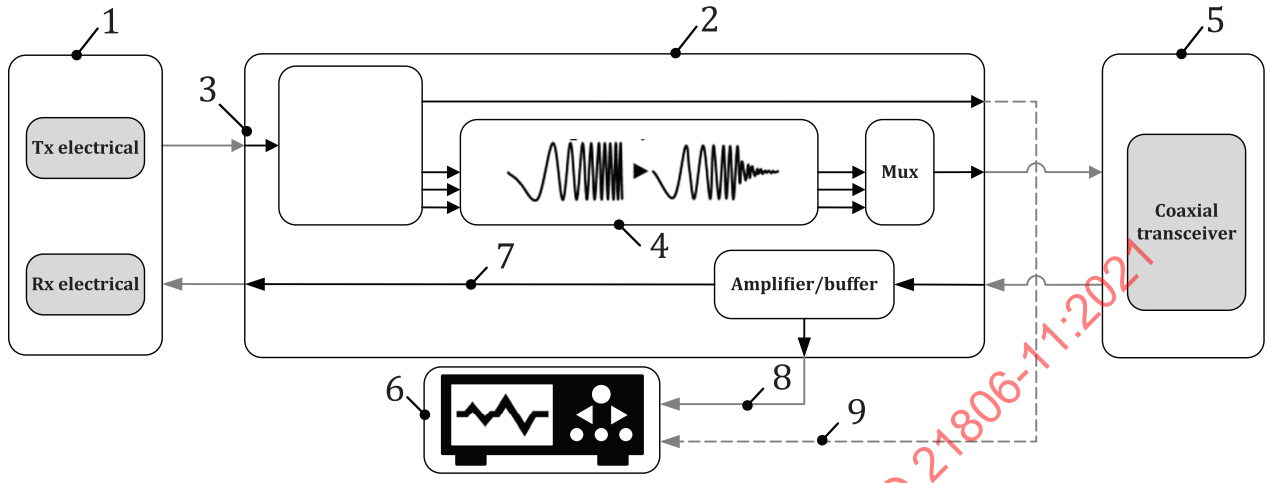
— oscilloscope.

The compensation set-up for MOST150 cPHY duplex is specified in Annex C and shall be followed. The status of Annex C is normative.

The test procedure for 2-port nodes is described in Annex D.

15.2 Test set-ups 1 and 2

Figure 65 shows the test set-up 1 simplex for limited physical layer conformance test.



Key

1 PHYSTT
2 MTCM
3 LVDS receiver multiplexer signal shaper
4 cable representations
5 IUT
6 oscilloscope
7 digital representation of receive pattern
8 analogue representation of receive pattern
9 reference for startup and shutdown timing measurement

Figure 65 — Test set-up 1 simplex for limited physical layer conformance test

Figure 66 shows the test set-up 2 duplex for limited physical layer conformance test.