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Road vehicles — Clock extension peripheral interface (CXPI) —

Part 7: Data link and physical layer conformance test plan

Véhicules routiers — Interface périphérique d'extension d'horloge (CXPI) —

Partie 7: Plan de test de conformité des couches de liaison de données et physique

Reference number
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Foreword

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The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

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For an explanation of the voluntary nature of standards, the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT), see www.iso.org/iso/foreword.html.

This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

A list of all parts in the ISO 20794 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Introduction

ISO 20794 (all parts) specifies the application (partly), application layer, transport layer, network layer, data link layer, and physical layer requirements of an in-vehicle network called clock extension peripheral interface (CXPI).

CXPI is an automotive low-speed single wire network. It is an enabler for reducing vehicle weight and fuel consumption by reducing wire counts to simple devices like switches and sensors.

CXPI serves as and is designed for automotive control applications, for example door control group, light switch and HVAC (Heating Ventilation and Air Condition) systems.

The CXPI services, protocols and their key characteristics are specified in different parts according to the OSI layers.

— Application and application layer:
  — application measurement and control data communication to exchange information between applications in different nodes based on message communication;
  — wake-up and sleep functionality;
  — two kinds of communication methods can be selected at system design by each node:
    i) the event-triggered method, which supports application measurement- and control-based (event-driven) slave node communication; and
    ii) the polling method, which supports slave node communication based on a periodic master schedule;
  — performs error detection and reports the result to the application;
  — application error management.
— Transport layer and network layer:
  — transforms a message into a single packet;
  — adds protocol control information for diagnostic and node configuration into each packet;
  — adds packet identifier for diagnostic and node configuration into each packet;
  — performs error detection and reports the result to higher OSI layers.
— Data link layer and physical layer:
  — provides long and short data frames;
  — adds a frame identifier into the frame;
  — adds frame information into the frame;
  — adds a cyclic redundancy check into the frame;
  — performs byte-wise arbitration and reports the arbitration result to higher OSI layers;
  — performs frame type detection in reception function;
  — performs error detection and reports the result to higher OSI layers;
  — performs Carrier Sense Multiple Access (CSMA);
  — performs Collision Resolution (CR);

— generates a clock, which is transmitted with each bit to synchronise the connected nodes on the CXPI network;

— supports bit rates up to 20 kbit/s.

To achieve this, it is based on the Open Systems Interconnection (OSI) Basic Reference Model specified in ISO/IEC 7498-1[1] and ISO/IEC 10731[2], which structures communication systems into seven layers.

Figure 1 illustrates an overview of communication frameworks beyond the scope of this document including related standards:

— vehicle normal communication framework, which is composed of ISO 20794-2, and ISO 20794-5[7];

— vehicle diagnostic communication framework, which is composed of ISO 14229-1[3], ISO 14229-2[4], and ISO 14229-8[5];

— presentation layer standards, e.g. vehicle manufacturer specific or ISO 22901-1 ODX[9];

— lower OSI layers framework, which is composed of ISO 20794-3[6], ISO 20794-4, ISO 20794-5, ISO 20794-6[8] and this document.

ISO 20794 (all parts) and ISO 14229-8[5] are based on the conventions specified in the OSI Service Conventions (ISO/IEC 10731[2]) as they apply for all layers and the diagnostic services.

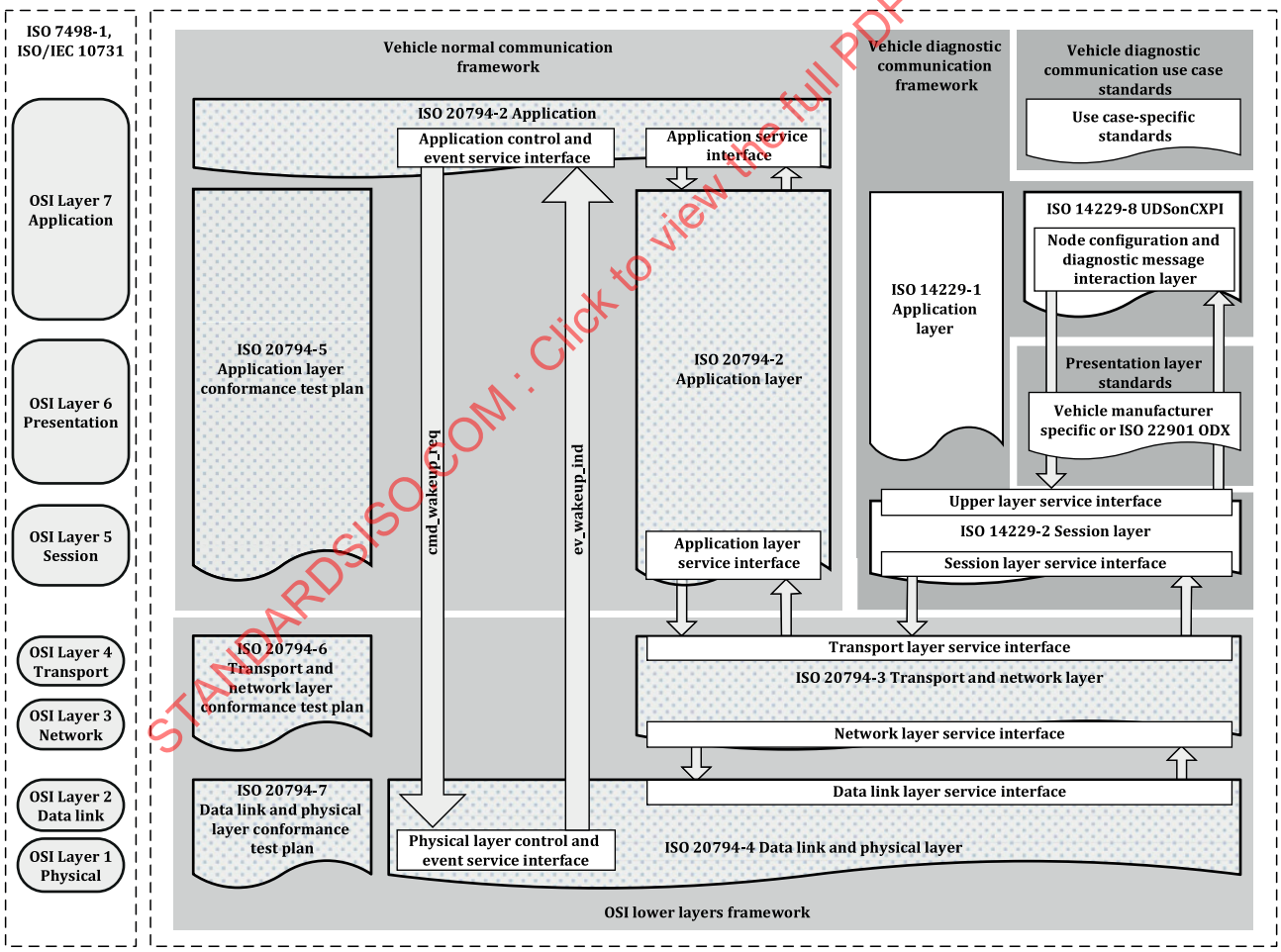


Figure 1 — ISO 20794 documents reference according to OSI model

Road vehicles — Clock extension peripheral interface (CXPI) —

Part 7: Data link and physical layer conformance test plan

1 Scope

This document specifies the conformance test plans for the CXPI data link layer and the CXPI physical layer. It also specifies the conformance test plan for error detection.

Additionally, this document describes the concept of conformance test plan operation.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 7498-1:1994, *Information processing systems — Open systems interconnection — Basic reference model*

ISO 20794-2:2020, *Road vehicles — Clock extension peripheral interface (CXPI) — Part 2: Application layer*

ISO 20794-4:2020, *Road vehicles — Clock extension peripheral interface (CXPI) — Part 4: Data link layer and physical layer*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 20794-2, ISO 20794-4 and ISO/IEC 7498-1 apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at http://www.electropedia.org/

4 Symbols and abbreviated terms

4.1 Symbols

---	empty cell/undefined
C_{BUS}	total bus capacitance
C_{PG}	capacity of pulse generator/data generator
C_{SLAVE}	capacity of slave node
kbit/s	kilobit per second

R_{MASTER}	master node resistor
R_{SLAVE}	slave node resistor
t_{bit}	bit time
$t_{rx\_dif\_cont}$	difference of the dominant time between logical value 1 and logical value 0
$t_{rx\_wakeup\_clk}$	time that the receiving clock master detects the width of dominant level as the wake-up pulse
t_{rx_wakeup}	time that the receiving node detects each width of dominant level in the wake-up pulse from first dominant pulse
$t_{rx\_wakeup\_space}$	limitation time of acceptance second dominant pulse in the wake-up pulse from first dominant pulse
t_{tx_wakeup}	time that the transceiver node transmits the dominant voltage of the wake-up pulse
$t_{tx\_wakeup\_space}$	interval time between two of dominant level of transmitting wake-up pulse
$t_{tx\_0\_lo}$	dominant time of logical value 0
$t_{tx\_0\_lo\_dom}$	dominant time of logical value 0 (TH_{tx_dom} = 30 % of V_{SUP})
$t_{tx\_0\_lo\_rec}$	dominant time of logical value 0 (TH_{tx_rec} = 70 % of V_{SUP})
$t_{tx\_0\_pd}$	at the time of logical value 0 outputs, time from the LO level detection of the CXPI network until falling the voltage TH_{tx_dom} = 30 % of V_{SUP}
$t_{tx\_1\_lo}$	dominant time of logical value 1
$t_{tx\_1\_lo\_dom}$	dominant time of logical value 1 (TH_{tx_dom} = 30 % of V_{SUP})
$t_{tx\_1\_lo\_rec}$	dominant time of logical value 1 (TH_{tx_rec} = 70 % of V_{SUP})
TH_{tx_dom}	dominant threshold voltage of the driver node
TH_{tx_rec}	recessive threshold voltage of the driver node
V_{BUS}	voltage of CXPI network
V_{BUS_CNT}	centre recessive threshold voltage of the received node
V_{HYS}	hysteresis voltage between the recessive threshold voltage and the dominant threshold voltage of the received node
V_{th_dom}	measured value of the dominant threshold voltage of the received node
V_{th_rec}	measured value of the recessive threshold voltage of the received node
V_{rec_master}	maximum recessive level of logical value 1

4.2 Abbreviated terms

AC	alternating current
CRC	cyclic redundancy check
DLC	data length code

DLL	data link layer
ECU	electronic control unit
FI	frame information
HI	high
IBS	inter byte space
ID	identifier
IFS	inter frame space
LO	low
N/A	not applicable
NM	network management
OSI	open systems interconnection
PID	protected identifier
PHY	physical layer
PMA	physical media attachment
PMD	physical media dependent
PS	physical signalling
PWM	pulse width modulation
RX_{PWM}	PMA receiver interface signal
SUT	system under test
TH	threshold
TX_{PWM}	PMA transmits interface signal
TYPE	frame type

5 Conventions

This document is based on OSI service conventions as specified in ISO/IEC 10731[2] and ISO/IEC 9646-1[1] for conformance test system set-up.

6 General test specification considerations

6.1 General

This document covers the conformance test cases (CTC) to verify the requirements described in ISO 20794-4:2020 data link layer and physical layer document.

6.2 Test conditions

Tests can be performed at room temperature, if the temperature is in the range of 15° C to 35° C. Also, the tests shall be performed under room EMI (electro-magnetic interference) conditions.

6.3 IUT requirements

The occurrence of the error specified in ISO 20794-2:2020, 9.6.8 shall be notified to the other nodes. IUT shall be initialised in the test case respectively.

6.4 CTC definition

The definition of each test case specifies, whether the IUT is a master or slave node. Each CTC is defined in the structure as defined in Table 1.

Table 1 — CTC definition example

Item	Content
CTC # – Title	[OSI layer #].CTC_[number_name] E.g. 2.CTC_2.6 – L_FI_DLC ≠ 1111_2 and frame data verification 2 if DLC is 1101_2 or 1110_2
Purpose	This CTC verifies that the DLC field for the frame of L_FI_DLC ≠ 1111_2 complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 2.10 DLL – L_FI_DLC (data length code); — REQ 2.30 DLL – Function models – DLL – Transmission logic; — REQ 2.31 DLL – Function models – DLL – Reception logic.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 (see 6.6.4) and in addition support TST_FRM_01_REQ_PID, TST_FRM_11_RESP_12, TST_FRM_05_REQ_PID_ERRBIT, and TST_FRM_18_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The LT shall transmit TST_FRM_01_REQ_PID and TST_FRM_11_RESP_12 changing the DLC value as specified in Table 22. 2. The IUT does not detect any error and reports the result to higher OSI layers. 3. The LT shall transmit TST_FRM_05_REQ_PID_ERRBIT (refer to remark 1). 4. The IUT transmits TST_FRM_05_REQ_PID_ERRBIT (refer to remark 2) and TST_FRM_18_RESP_ERRBIT_0-12. 5. The LT shall observe TST_FRM_18_RESP_ERRBIT_0-12 with the result of detect error bit on the CXPI network.
Iteration	Steps are executed for each test case specified in Table 22; REPEAT step 1 to step 5, 2 times; The LT shall set L_FI_DLC as specified in Table 22; REPEAT END.
Expected response	After step 1: The IUT receives TST_FRM_11_RESP_12 as 12 data bytes regardless of L_FI_DLC value. After step 4: The IUT transmits TST_FRM_18_RESP_ERRBIT_0-12 with the error bit = FALSE.

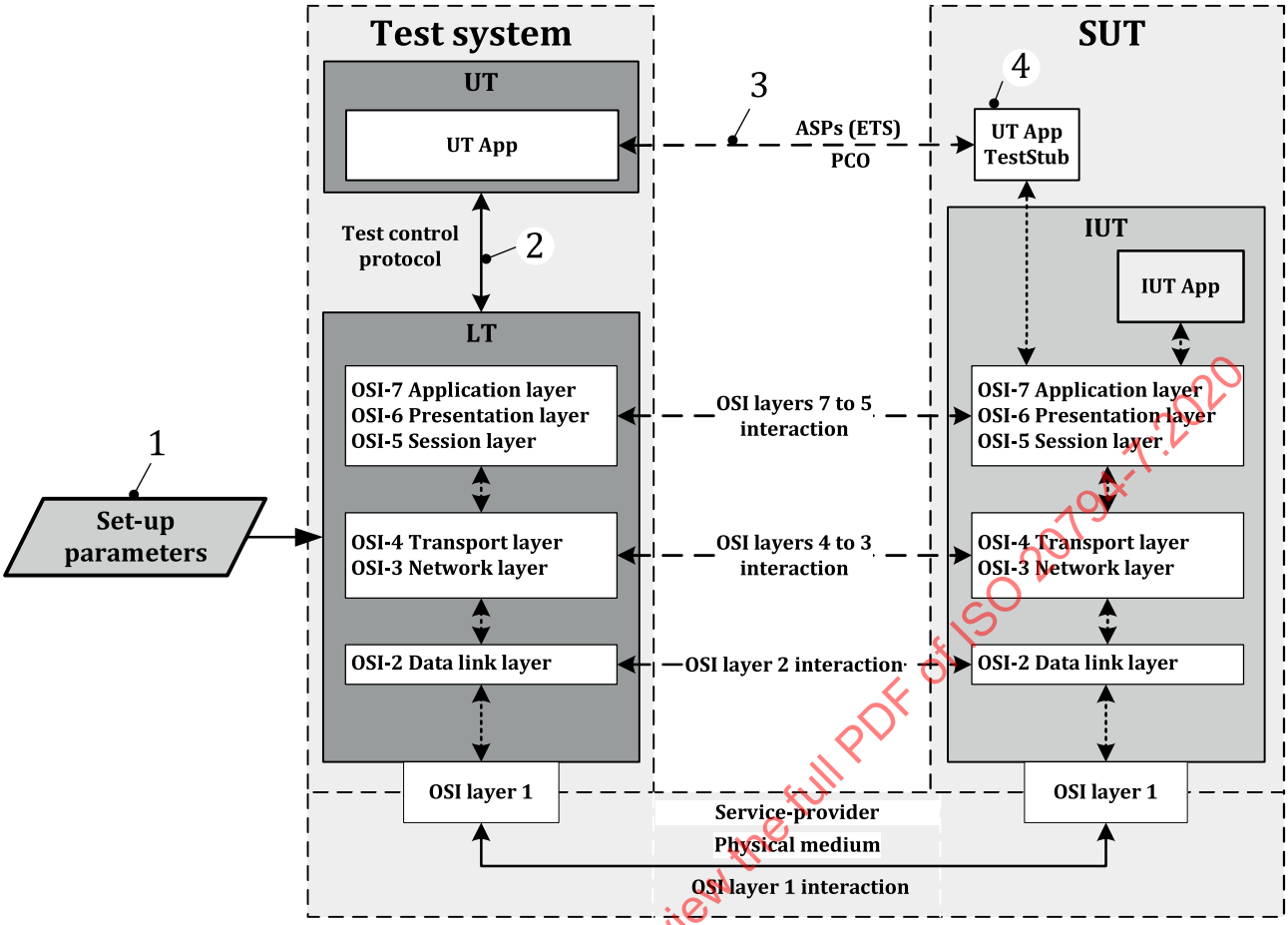
Table 1 *(continued)*

Item	Content
	After step 5: The LT shall receive TST_FRM_18_RESP_ERRBIT_0-12 with the error bit = FALSE.
Remark	1. If the IUT transmits the TST_FRM_18_RESP_ERRBIT_0-12 then the LT is expected to transmit this TST_FRM_05_REQ_PID_ERRBIT message. 2. Step 4 can be skipped if step 3 is required.

6.5 Test system set-up

The test system set-up follows the ISO/IEC 9646-1 and consists of a test system and a system under test (SUT) connected via the physical medium. The test system implements an UT and a LT. The UT uses the test control protocol (see Figure 2, key 2) to control the LT. The LT supports the functionality required to test the OSI layers (see Figure 2, key 4) of the IUT. The test system uses the IUT-specific set-up parameters (see Figure 2, key 1) for testing the communication with the IUT.

The control and measurement functionality is provided by direct access to the service interface (see Figure 2, key 3) and the associated parameters of the OSI layers as specified in the ISO 20794 series. The conformance test controller manipulates the service interface parameters of the OSI layers to fulfil the purpose of each conformance test case (CTC). The test system ensures the precision of the bit time and bit synchronisation of the master node as specified in ISO 20794-4:2020, 9.3.7. If the IUT is a master node then the LT functions as a slave node. If the IUT is a slave node then the LT functions as a master node.



Key

1 set-up parameters (CXPI node's electronic data sheet)

2 test control protocol

3 abstract service primitives (ASPs) based on enhanced testability services (ETS) and points of control and observation (PCO)

4 upper tester application test stub

Figure 2 — Test system set-up

6.6 Configuration of test system and IUT

6.6.1 General

The test system requires set-up parameters (see Figure 2 key 1), which specify data link layer and physical layer properties of the IUT. The IUT-specific data sheet (see Figure 2, key 1) includes set-up parameters, which the test system requires to perform the CTCs.

Table 2 specifies the configuration of test system and the IUT in the CTCs. In each CTC description, configuration is specified in the 'configuration' column.

Table 2 — Configuration of test system and IUT

Configuration item	Configuration of test system and IUT				
	Default	L_ErrDet1	L_ErrDet2	L_Arbit	L_Unknown
Request identifier by test system	N/A	N/A	N/A	Higher priority	N/A
L_PID	Any valid	Any valid	Any invalid	Any valid	Any invalid
IBS	Less than 9-bit length and more than 1-bit length				
TST_FRM_05_REQ_PID_ERRBIT	N/A	Use	Use	N/A	N/A

Table 3 specifies test message names, which are used by the IUT and the test system in the CTCs. In each CTC description, the message setting is specified in the 'description' column. The configuration described is a suitable configuration for each CTC. If there is no reference to Table 3, the settings are specified in the CTC.

If the IUT is not able to support the given FrameId, it is possible to replace the given FrameId with the FrameId that the IUT can handle.

All frames used are selected so that they should be valid for the IUT. If the specification does not specify the direction (transmission or reception) of frame transfer, the IUT shall have both transmission and reception ability in principle.

Table 3 — Configuration of test frame used by IUT and test system

Name	Definition
TST_FRM_00_REQ_PTYPE	Test frame 00_{16} of master node including a PtypeId value (00_{16}) of L_ReqId.
TST_FRM_01_REQ_PID	Test frame 01_{16} of master or slave node including an L_PID value (01_{16} to $7F_{16}$,) of L_ReqId.
TST_FRM_03_REQ_PID_UNKNOWN	Test frame 03_{16} of master or slave node including an unknown L_PID value of L_ReqId (not defined for reception/transmission by IUT).
TST_FRM_05_REQ_PID_ERRBIT	Test frame 05_{16} of master or slave node including an error bit L_PID value (01_{16} to $7F_{16}$,) of L_ReqId. The value of this PID can use supplier-specific ReqId ($3F_{16}$).
TST_FRM_10_RESP_0-12	Test frame 10_{16} of master or slave node including an FI field, DATA field and CRC field determined by $00_{16} \leq$ L_Length $\leq 0C_{16}$.
TST_FRM_12_RESP_LONG_0-255	Test frame 12_{16} of master or slave node including an FI field, DATA field and CRC field determined by $00_{16} \leq$ L_Length $\leq FF_{16}$.
TST_FRM_13_RESP_UNKOWN_0-12	Test frame 13_{16} of master or slave node including an FI field, DATA field and CRC field (not defined for reception/transmission by IUT) with a correct parity bit determined by $00_{16} \leq$ L_Length $\leq 0C_{16}$.
TST_FRM_16_RESP_ERRBIT_0-12	Test frame 16_{16} of master or slave node including an FI field, DATA field with an error bit and CRC field determined by $00_{16} \leq$ L_Length $\leq 0C_{16}$.

6.6.2 IUT-specific set-up parameters

The IUT-specific set-up parameters include at least the following information.

— The request identifier uses 01_{16} to $7F_{16}$ and uses 00_{16} in the request protected type identifier field. The useage of other values is invalid.

— The bit rate shall be set following each test case, and default bit rate is specified as 20 kbit/s.

— The delay between the L_PID field and response field shall comply with ISO 20794-4:2020, 8.6.1.

— If width of LO level of logical value 1 is maximum $t_{tx\_1\_lo\_rec\_TS} = 0{,}39\ t_{bit} + 0{,}6\ \tau$, then the test is done with $\tau = 5$.

— DID associated result parameter error information related to CXPI data link layer and CXPI physical layer.

6.6.3 Default configurations

The default parameters include at least the following information:

— L_PID: sets any valid value supported by IUT; and

— IBS: less than 9-bit length and more than 1-bit length.

6.6.4 L_ErrDet1 configurations

The L_ErrDet1 parameters include at least the following information:

— L_PID: sets any valid value supported by IUT;

— IBS: less than 9-bit length and more than 1-bit length; and

— TST_FRM_05_REQ_PID_ERRBIT: supported by IUT.

6.6.5 L_ErrDet2 configurations

The L_ErrDet2 parameters include at least the following information:

— L_PID: sets any invalid value;

— IBS: less than 9-bit length and more than 1-bit length; and

— TST_FRM_05_REQ_PID_ERRBIT: supported by IUT.

6.6.6 L_Arbit configurations

The L_Arbit parameters include at least the following information:

— L_PID: sets any valid value supported by IUT; and

— IBS: less than 9-bit length and more than 1-bit length.

6.6.7 L_Unknown configurations

The L_Unknown parameters include at least the following information:

— L_PID: sets any invalid value; and

— IBS: less than 9-bit length and more than 1-bit length.

6.7 SUT initialisation

An initialisation of the SUT shall be performed before each CTC, it is as follows:

— default initialisation – the IUT shall be reset so that the transmission/reception of L_ReqIds shall be configured and the error counter value is reset (to 0). If the IUT is a master node, it shall be ready to transmit the request field to the lower OSI layer. If the IUT is a slave node, it shall be ready to transmit response PDUs upon the reception of a L_ReqIds from the master node;

— L_PwrMng1 initialisation;

— SUT shall be powered off;

— L_PwrMng2 initialisation; and

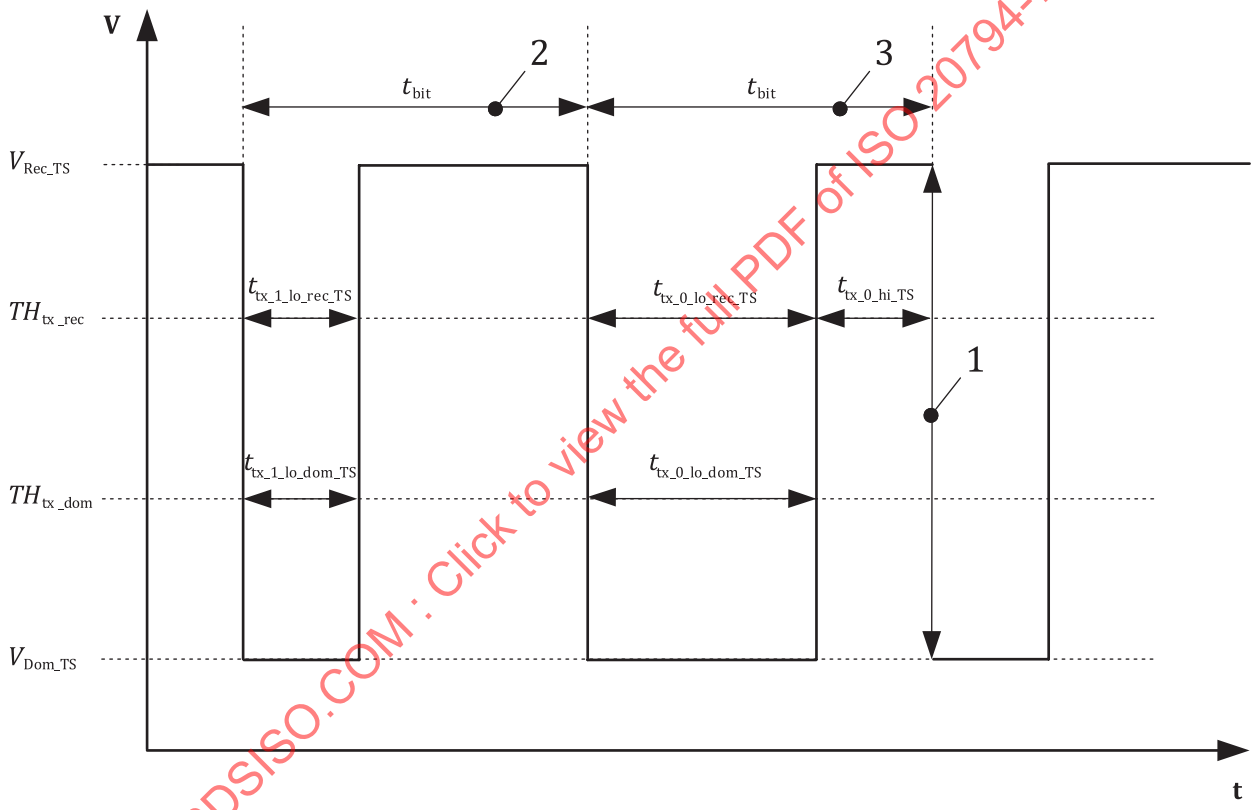
— SUT shall be powered, but the IUT shall not transmit and receive bits.

6.8 Additional test system set-up capabilities

6.8.1 CXPI network data generator

The CXPI network data generator as the test system shall be able to transmit CXPI frames with adjustable recessive/dominant levels, duty cycle of logical value 1 and 0.

Figure 3 shows an example of a CXPI waveform which the test system transmits. The dominant width (duty cycle) $t_{tx\_1\_lo\_dom\_TS}$ and $t_{tx\_0\_lo\_dom\_TS}$ of the logical value 1 and 0 waveform or the recessive width (duty cycle) $t_{rx\_0\_hi\_TS}$ of the logical value 0 waveform are defined in each test. If there is no definition for each test, it shall comply with Table 4. To be $t_{tx\_1\_lo\_dom\_TS} \approx t_{tx\_1\_lo\_rec\_TS}$ and $t_{tx\_0\_lo\_dom\_TS} \approx t_{tx\_0\_lo\_rec\_TS}$, the rising and falling edge shall set as sharp as possible.



Key

1 amplitude (signal voltage)
2 t_{bit} logical value 1
3 t_{bit} logical value 0
V voltage
t time

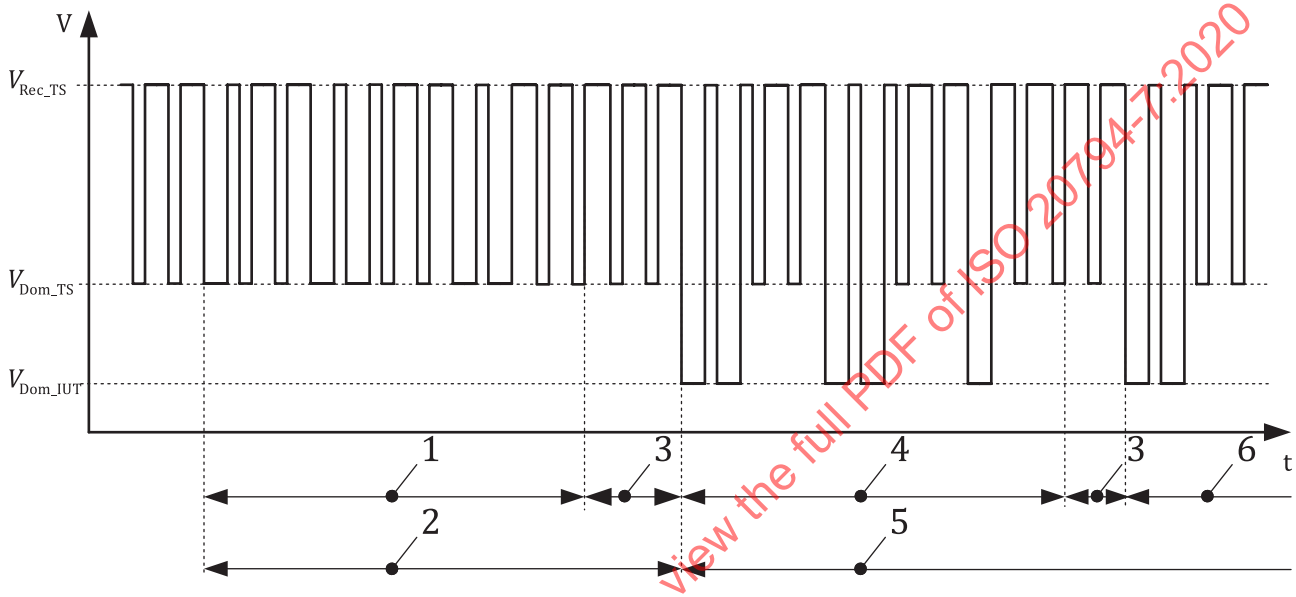
Figure 3 — PWM signal

Table 4 defines the typical value of the dominant time (the logical value 1 and 0).

Table 4 — Typical value of dominant time (logical value 1 and 0)

$t_{tx\_1\_lo\_dom\_TS}$ (LO width of logical value 1)	$t_{tx\_0\_lo\_dom\_TS}$ (LO width of logical value 0)
12,5 µs ±10 % (at t_{bit}=20 kbit/s)	35 µs ±10 % (at t_{bit}=20 kbit/s)

Figure 4 shows an example of the test system as master node transmits the L_PID field which is adjusted the dominant voltage (V_{Dom_TS}) and the IUT as a slave node transmits response by the nominal dominant voltage value (V_{Dom_IUT}).

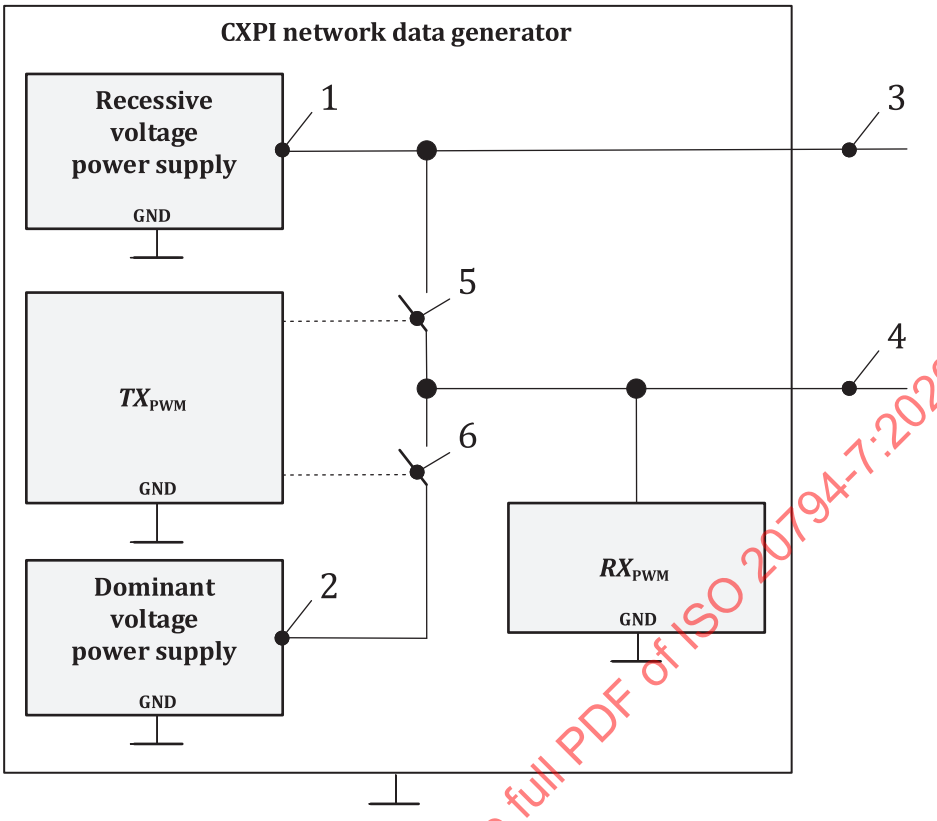


Key

1 L_PID field
2 transmission by test system as master node
3 IBS
4 frame information
5 transmission by IUT as slave node
6 data 1
V voltage
t time

Figure 4 — Example of test system as master node and IUT as slave node dominant voltage behaviour

The test system shall be able to transmit the L_PID field or the response field. It also shall be able to change the response dynamically according to the CXPI frame received. The CXPI network data generator test set-up is shown in Figure 5.



Key

1 V_{Rec_TS}
2 V_{Dom_TS}
3 $V_{Pull\text{-}up}$
4 CXPI network
5 switch 1
6 switch 2

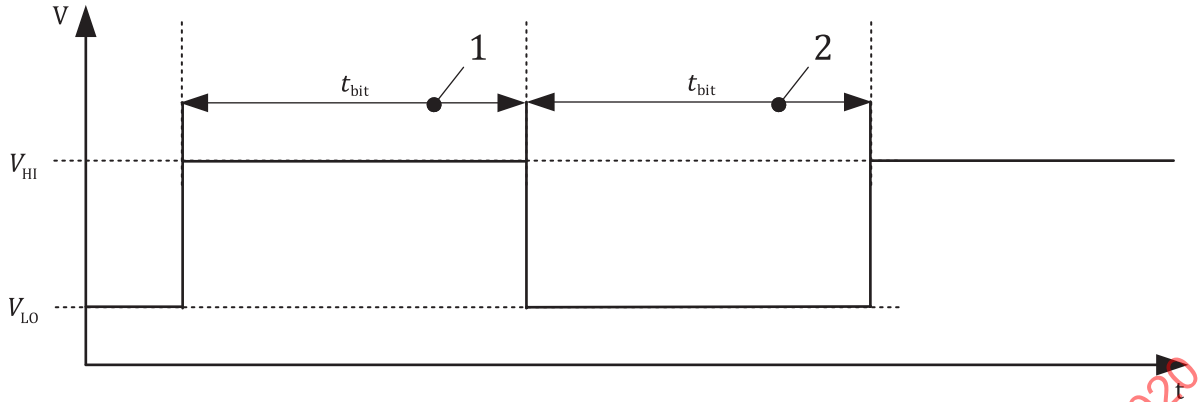
Figure 5 — CXPI network data generator test set-up

The CXPI network data generator includes the two power supply devices which provide the dominant voltage (V_{Dom_TS}) and recessive voltage (V_{Rec_TS}) to transmit the CXPI frame. CXPI network data generator shall be able to transmit the recessive voltage by connecting the CXPI network to the recessive voltage power via low impedance pass (switch 1). The V_{Dom_TS} and $V_{Rec\_TS}/V_{Pull\text{-}up}$ are defined for each test where CXPI network data generator is used.

6.8.2 *TXD* data generator

The *TXD* data generator as the test system shall be able to transmit frames with a logical value of 1 and a logical value of 0.

Figure 6 shows an example of a waveform which the test system transmits. The waveform of *TXD* is formed by non-return to zero. Configure the rise/fall time of the waveform as short as possible.

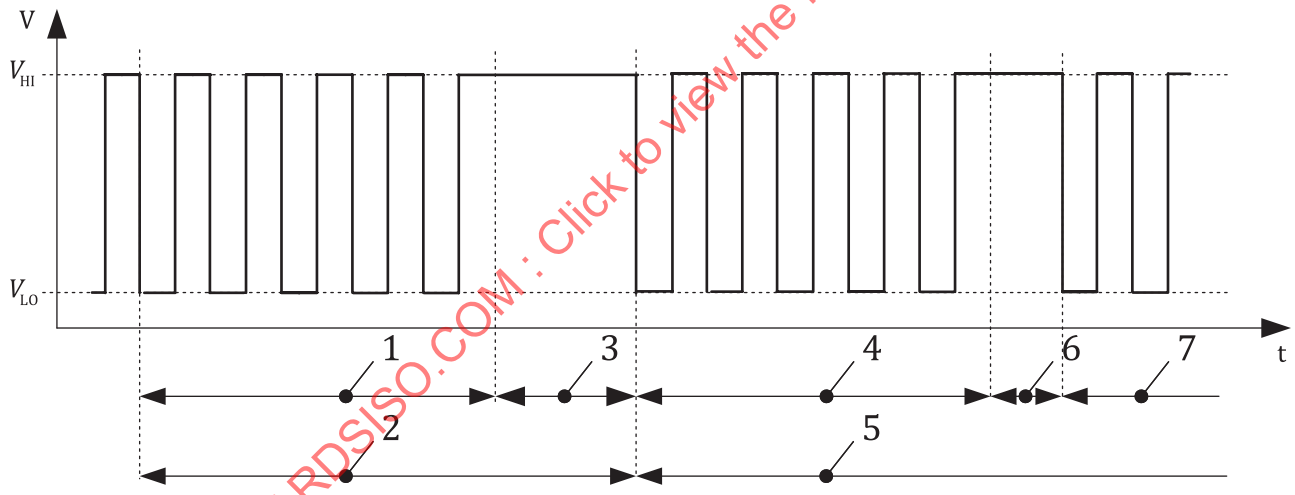


Key

1 t_{bit} logical value of 1
2 t_{bit} logical value of 0
V voltage
t time

Figure 6 — *TXD* signal

An example of L_PID field and response field transmitted to IUT from *TXD* data generator is shown in Figure 7.

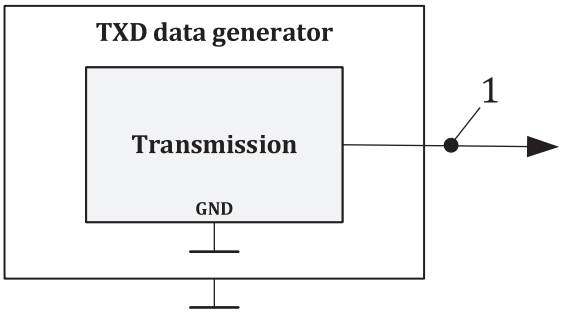


Key

1 L_PID field
2 transmission by test system as master node
3 IBS (4 bit)
4 frame information
5 transmission by IUT as slave node
6 IBS (2 bit)
7 data 1
V voltage
t time

Figure 7 — Operation example

The *TXD* data generator for test set-up is shown in Figure 8.



Key

1 *TXD*

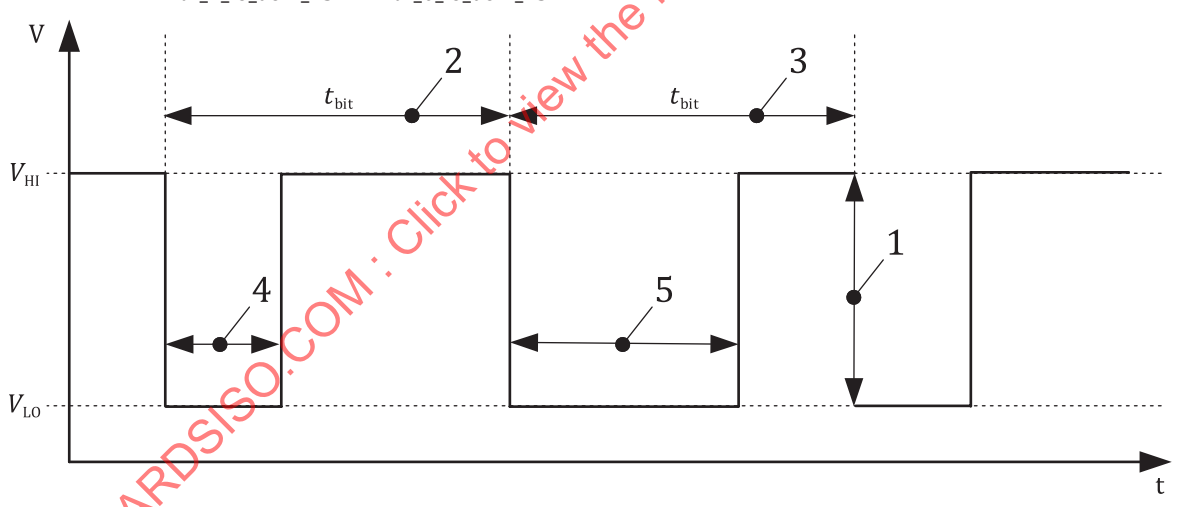
Figure 8 — *TXD* data generator test set-up

The *TXD* data generator transmits data within the range of voltage V_{HI} and V_{LO}.

6.8.3 TX_{PWM} data generator

The TX_{PWM} data generator as the test system shall be able to transmit the CXPI frames with adjustable V_{HI}/V_{LO} levels, duty cycle of logical value 1 and 0.

Figure 9 shows an example of the TX_{PWM} waveform. The width (t_{bit}) of a logical value 1 and 0 waveform is determined by $D_{tx\_1\_lo\_dom\_TS}$ or $D_{tx\_0\_lo\_dom\_TS}$. All CTCs shall be in accordance with Table 6.



Key

1 amplitude (signal voltage)
2 t_{bit} logical value 1
3 t_{bit} logical value 0
4 $t_{tx\_1\_lo\_dom\_TS}$
5 $t_{tx\_0\_lo\_dom\_TS}$
V voltage
t time

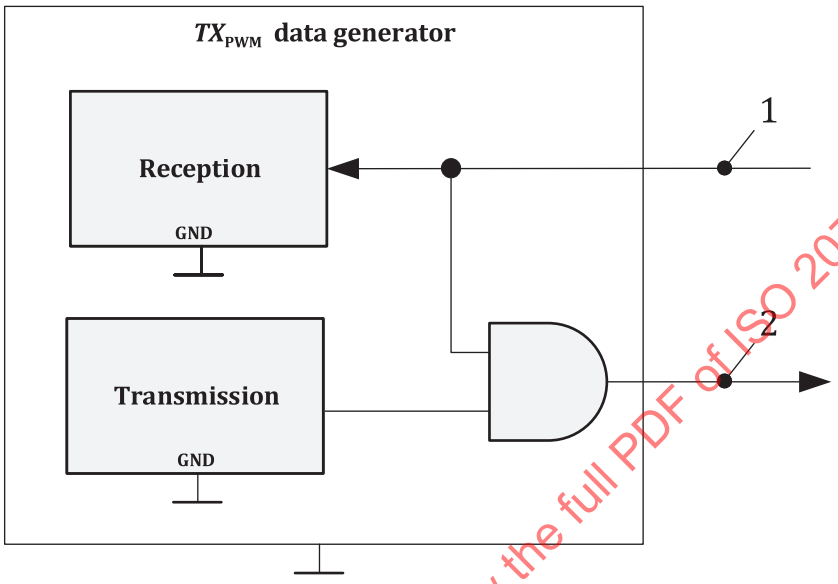
Figure 9 — TX_{PWM} signal

Table 5 defines the typical value of the dominant time (the logical value 1 and 0).

Table 5 — Typical value of dominant time (logical value 1 and 0)

$D_{tx\_1\_lo\_dom\_TS}$ (LO width of logical value 1)	$D_{tx\_0\_lo\_dom\_TS}$ (LO width of logical value 0)
(12,5 ± 1,25) µs (at t_{bit}=20 kbit/s)	(35 ± 3,5) µs (at t_{bit}=20 kbit/s)

The TX_{PWM} data generator for test set-up is shown in Figure 10.



Key

1 RX_{PWM}
2 TX_{PWM}
3 logical gate AND

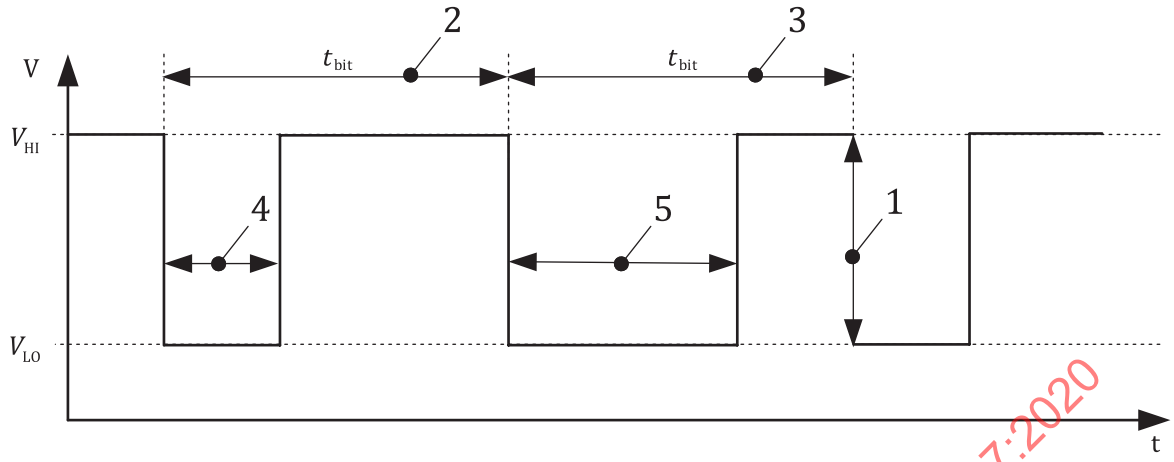
Figure 10 — TX_{PWM} data generator test set-up

The TX_{PWM} data generator includes the transmission and reception. When RX_{PWM} is logical value 1, the TX_{PWM} data generator outputs PWM waveform.

6.8.4 RX_{PWM} data generator

The RX_{PWM} data generator as the test system shall be able to transmit the CXPI frames with adjustable V_{HI}/V_{LO} levels, duty cycle of alogical value 1 and 0.

Figure 11 shows an example of a RX_{PWM} waveform. The width (t_{bit}) of a logical value 1 and 0 waveform is determined by $D_{tx\_1\_lo\_dom\_TS}$ or $D_{tx\_0\_lo\_dom\_TS}$. All CTCs shall be in accordance with Table 6.



Key

1 amplitude (signal voltage)
2 t_{bit} logical value 1
3 t_{bit} logical value 0
4 $t_{tx\_1\_lo\_dom\_TS}$
5 $t_{tx\_0\_lo\_dom\_TS}$
V voltage
t time

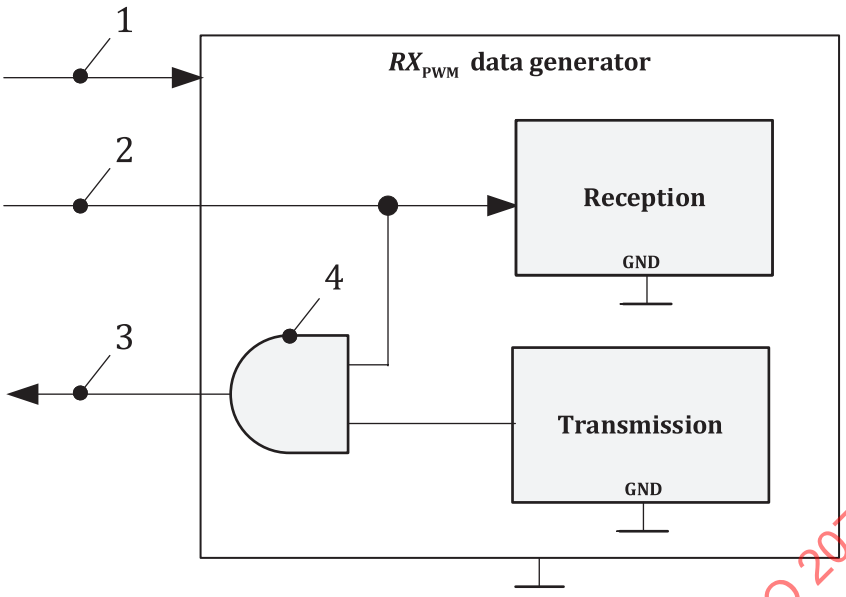
Figure 11 — RX_{PWM} signal

Table 6 defines the typical value of the dominant time (the logical value 1 and 0).

Table 6 — Typical value of dominant time (logical value 1 and 0)

$t_{tx\_1\_lo\_dom\_TS}$ (LO width of logical value 1)	$t_{tx\_0\_lo\_dom\_TS}$ (LO width of logical value 0)
12,5 µs ±10 % (at t_{bit}=20 kbit/s)	35 µs ±10 % (at t_{bit}=20 kbit/s)

The RX_{PWM} data generator for the test set-up is shown in Figure 12.



Key

1 *TXD* (for synchronisation of the *TXD* data generator)
2 TX_{PWM}
3 RX_{PWM}
4 logical gate "AND"

Figure 12 — RX_{PWM} data generator test set-up

The RX_{PWM} data generator includes the transmission and reception. When the TX_{PWM} has a logical value 1, the RX_{PWM} data generator outputs the PWM waveform.

6.8.5 Other requirements

Table 7 specifies the line characteristics requirements.

Table 7 — Line characteristics requirements

Line characteristics range	Description
$1 \leq \tau \leq 5$[a]	Time constant of the entire system τ
[a] If the width of the LO level of the logical value 1 is minimum $t_{tx\_1\_lo\_dom\_TS} = 0{,}11\ t_{bit}$, then the test shall be done with $\tau = 1$. If the width of the LO level of the logical value 1 is maximum $t_{tx\_1\_lo\_rec\_TS} = 0{,}39\ t_{bit} + 0{,}6\ \tau$, then the test shall be done with τ = 5.	

7 Data link layer conformance test plan

7.1 General

The data link layer conformance test evaluates the operation of the response field (L_PDU), whether those are transmitted and received in the correct order according to ISO 20794-4. This conformance test only covers the data link layer service functionality.

7.2 CTP – Timing parameters

7.2.1 2.CTC_1.1 – IBS length

Table 8 specifies the CTC that verifies the 2.CTC_1.1 – IBS length.

Table 8 — 2.CTC_1.1 – IBS length

Item	Content
CTC # – Title	2.CTC_1.1 – IBS length
Purpose	This CTC verifies that the length of the IBS complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 2.19 DLL – Internal operation – Unsegmented frame; — REQ 2.20 DLL – Internal operation – Frame serialisation and bit order; — REQ 2.21 DLL – IBS timing handling.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to default configurations (see 6.6.3) and in addition support TST_FRM_00_REQ_PTYPE, TST_FRM_01_REQ_PID and TST_FRM_10_RESP_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to transmit the TST_FRM_00_REQ_PTYPE (see remark 1), the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12.
Iteration	Not applicable
Expected response	After step 1: The LT shall observe an IBS between the TST_FRM_00_REQ_PTYPE and the TST_FRM_01_REQ_PID, which is more than 1-bit in length and less than 9-bit in length. The LT shall observe an IBS between the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12, which is more than 1-bit in length and less than 9-bit in length. The LT shall observe IBS between each byte of the TST_FRM_10_RESP_0-12, which is more than 1-bit in length and less than 9-bit in length.
Remark	1. The TST_FRM_00_REQ_PTYPE is only applicable to the IUTs which support polling method.

7.2.2 2.CTC_1.2 – IFS length

Table 9 specifies the CTC that verifies the 2.CTC_1.2 – IFS length.

Table 9 — 2.CTC_1.2 – IFS length

Item	Content
CTC # – Title	2.CTC_1.2 – IFS length
Purpose	This CTC verifies that the length of the IFS complies with the CXPI specification. This CTC is applicable only to an IUT, which support the L_PID field transmission.
Reference	ISO 20794-4:2020, REQ 2.22 DLL – IFS timing handling.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to default configurations (see 6.6.3) and in addition support TST_FRM_01_REQ_PID. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to transmit the TST_FRM_01_REQ_PID during any other frame transmission.
Iteration	Not applicable

Table 9 *(continued)*

Item	Content	
Expected response	After step 1:	The LT shall observe an IFS between the TST_FRM_01_REQ_PID and any other frame transmission, which is more than 20-bit in length.
Remark	---	

7.2.3 2.CTC_1.3 – Frame reception starting condition 1 without the error bit

Table 10 specifies the CTC that verifies the 2.CTC_1.3 – Frame reception starting condition 1 without the error bit.

Table 10 — 2.CTC_1.3 – Frame reception starting condition 1 without the error bit

Item	Content
CTC # – Title	2.CTC_1.3 – Frame reception starting condition 1 without the error bit
Purpose	This CTC verifies that the starting condition of a frame reception complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 2.23 DLL – Beginning condition of frame.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to default configurations (see 6.6.3) and in addition support TST_FRM_01_REQ_PID and TST_FRM_10_RESP_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12. 2. The LT shall transmit the TST_FRM_01_REQ_PID with 11-bit IFS interval, to make the IUT transmits the TST_FRM_10_RESP_0-12.
Iteration	Not applicable
Expected response	After step 2: The IUT shall transmit the TST_FRM_10_RESP_0-12. The LT shall receive the TST_FRM_10_RESP_0-12 and shall report to the UT.
Remark	---

7.2.4 2.CTC_1.4 – Frame reception starting condition 1 with the error bit

Table 11 specifies the CTC that verifies the 2.CTC_1.4 – Frame reception starting condition 1 with the error bit.

Table 11 — 2.CTC_1.4 – Frame reception starting condition 1 with the error bit

Item	Content
CTC # – Title	2.CTC_1.4 – Frame reception starting condition 1 with the error bit
Purpose	This CTC verifies that the starting condition of the frame reception complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 2.23 DLL – Beginning condition of frame.
Prerequisite	The test system set-up shall be in accordance with Figure 2.

Table 11 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.3) and in addition support TST_FRM_01_REQ_PID, TST_FRM_10_RESP_0-12, TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12. 2. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12 with 11-bit IFS interval. 3. The LT shall transmit the TST_FRM_05_REQ_PID.
Iteration	Not applicable
Expected response	After step 2: The IUT shall receive the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12. After step 3: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE and shall report to the UT.
Remark	---

7.2.5 2.CTC_1.5 – Frame reception starting condition 2 without the error bit

Table 12 specifies the CTC that verifies the 2.CTC_1.5 – Frame reception starting condition 2 without the error bit.

Table 12 — 2.CTC_1.5 – Frame reception starting condition 2 without the error bit

Item	Content
CTC # – Title	2.CTC_1.5 – Frame reception starting condition 2 without the error bit
Purpose	This CTC verifies that the starting condition of the frame reception complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 2.23 DLL – Beginning condition of frame.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to default configurations (see 6.6.3) and in addition support TST_FRM_01_REQ_PID and TST_FRM_10_RESP_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12. 2. The LT shall transmit the TST_FRM_01_REQ_PID with a 9-bit IFS interval, to make the IUT transmits the TST_FRM_10_RESP_0-12.
Iteration	Not applicable
Expected response	After step 2: The IUT shall not transmit the TST_FRM_10_RESP_0-12. The LT shall not receive the TST_FRM_10_RESP_0-12.
Remark	---

7.2.6 2.CTC_1.6 – Frame reception starting condition 2 with the error bit

Table 13 specifies the CTC that verifies the 2.CTC_1.6 – Frame reception starting condition 2 with the error bit.

Table 13 — 2.CTC_1.6 – Frame reception starting condition 2 with the error bit

Item	Content
CTC # – Title	2.CTC_1.6 – Frame reception starting condition 2 with the error bit
Purpose	This CTC verifies that the starting condition of the frame reception complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 2.23 DLL – Beginning condition of frame.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.3) and in addition support TST_FRM_01_REQ_PID, TST_FRM_10_RESP_0-12, TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12. 2. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12 with a 9-bit IFS interval. 3. The LT shall transmit the TST_FRM_05_REQ_PID.
Iteration	Not applicable
Expected response	After step 2: The IUT shall not receive the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12. After step 3: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE and shall report to the UT.
Remark	---

7.2.7 2.CTC_1.7 – Frame reception starting condition 3

Table 14 specifies the CTC that verifies the 2.CTC_1.7 – Frame reception starting condition 3.

Table 14 — 2.CTC_1.7 – Frame reception starting condition 3

Item	Content
CTC # – Title	2.CTC_1.7 – Frame reception starting condition 3
Purpose	This CTC verifies that the starting condition of the frame reception complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 2.23 DLL – Beginning condition of frame.
Prerequisite	The test system set-up shall be in accordance with Figure 2.

Table 14 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.4) and in addition support TST_FRM_01_REQ_PID, TST_FRM_10_RESP_0-12, TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to L_PwrMng1 (see 6.7).
Step	1. The LT shall transmit the consecutive frames of the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12 included the CRC error with a 10-bit IFS interval. If the IUT is a master node it shall prepare to transmit the test frame with a 10-bit IFS interval immediately after it receives the clock waveform, it shall be the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12 included the CRC error. 2. The SUT shall be powered. 3. The LT shall transmit at least one the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12 after completing the power-on and initialisation process of the IUT. 4. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT in the interval of 20-bit of the IFS.
Iteration	Not applicable
Expected response	After step 4: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE and shall report to the UT.
Remark	---

7.2.8 2.CTC_1.8 – Maximum length of the frame

Table 15 specifies the CTC that verifies the 2.CTC_1.8 – Maximum length of the frame.

Table 15 — 2.CTC_1.8 – Maximum length of the frame

Item	Content
CTC # – Title	2.CTC_1.8 – Maximum length of the frame
Purpose	This CTC verifies that the maximum length of the frame complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 2.25 DLL – Frame transmission time.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to default configurations (see 6.6.3) and in addition support TST_FRM_01_REQ_PID, TST_FRM_10_RESP_0-12 and TST_FRM_12_RESP_LONG_0-255. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to transmit each TST_FRM_01_REQ_PID and TST_FRM_10_RESP_0-12. 2. The UT shall control the IUT to transmit each TST_FRM_01_REQ_PID and TST_FRM_12_RESP_LONG_0-255 (see remark 1).
Iteration	Not applicable

Table 15 *(continued)*

Item	Content
Expected response	After step 1: The IUT shall transmit the maximum value of the frame length which is less than or equal to (30 + (10 × data length)) ×1,9 bits in length. The LT shall receive the maximum value of the frame length which is less than or equal to (30 + (10 × data length)) ×1,9 bits in length and shall report to the UT. After step 2: The IUT shall transmit the maximum value of the frame length which is less than or equal to (50 + (10 × data length)) ×1,9 bits in length. The LT shall receive the maximum value of the frame length which is less than or equal to (50 + (10 × data length)) ×1,9 bits in length and shall report to the UT.
Remark	1. The TST_FRM_01_REQ_PID and the TST_FRM_13_RESP_LONG_0-255 is only applicable to the IUTs which support a frame of the L_FI_DLC = 1111_2.

7.3 CTP – Frame transmission/reception

7.3.1 2.CTC_2.1 – Response to L_PID field

Table 16 specifies the CTC that verifies the 2.CTC_2.1 – Response to L_PID field.

Table 16 — 2.CTC_2.1 – Response to L_PID field

Item	Content
CTC # – Title	2.CTC_2.1 – Response to L_PID field
Purpose	This CTC verifies that the IUT responds to the L_PID field with the proper frame format.
Reference	ISO 20794-4:2020: — REQ 2.5 DLL – Frame field definition; — REQ 2.7 DLL – Request identifier field; — REQ 2.8 DLL – L_PTYPE and L_PID parity determination; — REQ 2.12 DLL – DLL – L_FI_NM (network management); — REQ 2.13 DLL – L_FI_SCT (sequence count); — REQ 2.14 DLL – L_DATA (data field); — REQ 2.15 DLL – L_DATA (data field) – Big endian; — REQ 2.24 DLL – Start of frame; — REQ 2.27 DLL – Completing condition of L_PID field; — REQ 2.30 DLL – Function models – DLL – Transmission logic; — REQ 2.31 DLL – Function models – DLL – Reception logic.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to default configurations (see 6.6.3) and in addition support TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The LT shall transmit the TST_FRM_01_REQ_PID for the IUT to transmit the TST_FRM_10_RESP_0-12.
Iteration	Not applicable

Table 16 *(continued)*

Item	Content	
Expected response	After step 1:	The IUT shall transmit the TST_FRM_10_RESP_0-12 which complies with ISO 20794-4:2020, 8.4.1. The LT shall receive the TST_FRM_10_RESP_0-12 which complies with ISO 20794-4:2020, 8.4.1 and shall report to the UT.
Remark	---	

7.3.2 2.CTC_2.2 – L_PID field transmission

Table 17 specifies the CTC that verifies the 2.CTC_2.2 – L_PID field transmission.

Table 17 — 2.CTC_2.2 – L_PID field transmission

Item	Content
CTC # – Title	2.CTC_2.2 – L_PID field transmission
Purpose	This CTC verifies that the L_PID field transmitted by the IUT. This CTC is applicable only to an IUT, which supports the L_PID field transmission.
Reference	ISO 20794-4:2020: — REQ 0.3 SIP – ReqId, request identifier; — REQ 2.5 DLL – Frame field definition; — REQ 2.7 DLL – Request identifier field; — REQ 2.8 DLL – L_PTYPE and L_PID parity determination; — REQ 2.27 DLL – Completing condition of L_PID field; — REQ 2.30 DLL – Function models – DLL – Transmission logic.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to default configurations (see 6.6.3) and in addition support TST_FRM_01_REQ_PID. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	The UT shall control the IUT to transmit the TST_FRM_01_REQ_PID.
Iteration	Not applicable
Expected response	After step 1: The IUT shall transmit the formats of the L_PID field which complies with ISO 20794-4:2020, 8.4.2. LT shall receive the TST_FRM_01_REQ_PID and shall report to the UT.
Remark	---

7.3.3 2.CTC_2.3 – L_PTYPE field transmission

Table 18 specifies the CTC that verifies the 2.CTC_2.3 – L_PTYPE field transmission.

Table 18 — 2.CTC_2.3 – L_PTYPE field transmission

Item	Content
CTC # – Title	2.CTC_2.3 – L_PTYPE field transmission
Purpose	This CTC verifies that the L_PTYPE field transmitted by the IUT. This CTC is applicable only to an IUT, which support L_PTYPE field transmission.
Reference	ISO 20794-4:2020: — REQ 0.4 SIP – ReqTypeId, request type identifier; — REQ 2.6 DLL – Request type identifier field; — REQ 2.26 DLL – Completing condition of L_PTYPE field; — REQ 2.30 DLL – Function models – DLL – Transmission logic.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node. — The IUT shall be configured to default configurations (see 6.6.3) and in addition support TST_FRM_00_REQ_PTYPE. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to transmit the TST_FRM_00_REQ_PTYPE.
Iteration	Not applicable
Expected response	After step 1: The IUT shall transmit the format of the L_PTYPE field which complies with ISO 20794-4:2020, 8.4.2.1. The LT shall receive the TST_FRM_00_REQ_PTYPE and shall report to the UT.
Remark	---

7.3.4 2.CTC_2.4 – L_PTYPE field response function

Table 19 specifies the CTC that verifies the 2.CTC_2.4 – L_PTYPE field response function.

Table 19 — 2.CTC_2.4 – L_PTYPE field response function

Item	Content
CTC # – Title	2.CTC_2.4 – L_PTYPE field response function
Purpose	This CTC verifies that the IUT as a slave node responds to the L_PTYPE field. This CTC is applicable only to an IUT, which supports the L_PTYPE field response.
Reference	ISO 20794-4:2020:
	— REQ 2.6 DLL – Request type identifier field; — REQ 2.26 DLL – Completing condition of L_PTYPE field; — REQ 2.30 DLL – Function models – DLL – Transmission logic; — REQ 2.31 DLL – Function models – DLL – Reception logic.
Prerequisite	The test system set-up shall be in accordance with Figure 2.

Table 19 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.4) and in addition support TST_FRM_00_REQ_PTYPE, TST_FRM_01_REQ_PID, TST_FRM_10_RESP_0-12, TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12. 2. The LT shall transmit the TST_FRM_00_REQ_PTYPE. 3. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT. 4. The UT shall control the IUT not to transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12. 5. The LT shall retransmit the TST_FRM_00_REQ_PTYPE.
Iteration	Not applicable
Expected response	After step 1: The IUT shall transmit the TST_FRM_01_REQ_PID, the frame information, the Data and the CRC. The LT shall receive the TST_FRM_01_REQ_PID, the frame information, the Data and the CRC and shall report to the UT. After step 3: The IUT shall transmit the TST_FRM_18_RESP_ERRBIT_0-12 with the error bit = FALSE. The LT shall receive the TST_FRM_18_RESP_ERRBIT_0-12 with the error bit = FALSE and shall report to the UT. After step 5: The IUT shall not transmit the TST_FRM_01_REQ_PID. The LT shall not receive the TST_FRM_01_REQ_PID.
Remark	---

7.3.5 2.CTC_2.5 – L_FI_DLC ≠ 1111_2 and frame data verification 1

Table 20 specifies the CTC that verifies the 2.CTC_2.5 – L_FI_DLC ≠ 1111_2 and frame data verification 1.

Table 20 — 2.CTC_2.5 – L_FI_DLC ≠ 1111_2 and frame data verification 1

Item	Content
CTC # – Title	2.CTC_2.5 – L_FI_DLC ≠ 1111_2 and frame data verification 1
Purpose	This CTC verifies that the DLC field for the frame of the L_FI_DLC ≠ 1111_2 complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 0.5 SIP – PDU, protocol data unit; — REQ 0.6 SIP – Length, length of PDU; — REQ 2.9 DLL – L_FI configuration; — REQ 2.10 DLL – L_FI_DLC (data length code); — REQ 2.30 DLL – Function models – DLL – Transmission logic.
Prerequisite	The test system set-up shall be in accordance with Figure 2.

Table 20 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to default configurations (see 6.6.3) and in addition support TST_FRM_01_REQ_PID and TST_FRM_10_RESP_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12 changing the L_FI_DLC with all possible data length values.
Iteration	REPEAT step 1 up to the maximum value of the L_FI_DLC; UT in IUT shall change the L_FI_DLC according to the data length of the test frame; REPEAT END.
Expected response	After step 1: The IUT shall transmit the format of frame information which complies with ISO 20794-4:2020, 8.4.3.1. The IUT shall transmit the correlation between the L_FI_DLC value and the data length (size of the data byte) which complies with ISO 20794-4:2020, 8.4.3.2. The LT shall receive the format of frame information which complies with ISO 20794-4:2020, 8.4.3.1. The LT shall receive the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12 changing the L_FI_DLC with all possible data length values and shall report to the UT.
Remark	---

7.3.6 2.CTC_2.6 – L_FI_DLC ≠ 1111_2 and frame data verification 2 if DLC is 1101_2 or 1110_2 (Ftype = NormalCom)

Table 21 specifies the CTC that verifies the 2.CTC_2.6 – L_FI_DLC ≠ 1111_2 and frame data verification 2 if DLC is 1101_2 or 1110_2.

Table 21 — 2.CTC_2.6 – L_FI_DLC ≠ 1111_2 and frame data verification 2 if DLC is 1101_2 or 1110_2

Item	Content
CTC # – Title	2.CTC_2.6 – L_FI_DLC ≠ 1111_2 and frame data verification 2 if DLC is 1101_2 or 1110_2
Purpose	This CTC verifies that the DLC field for the frame of L_FI_DLC ≠ 1111_2 complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 2.10 DLL – L_FI_DLC (data length code); — REQ 2.30 DLL – Function models – DLL – Transmission logic; — REQ 2.31 DLL – Function models – DLL – Reception logic.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.4) and in addition support TST_FRM_01_REQ_PID, TST_FRM_10_RESP_0-12 (only L_Length = $0C_{16}$), TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).

Table 21 *(continued)*

Item	Content	
Step	1. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12 changing the DLC value as specified in Table 22. 2. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT.	
Iteration	Steps are executed for each test case specified in Table 22; REPEAT step 1 to step 2, 2 times; The LT shall set the L_FI_DLC as specified in Table 22; REPEAT END.	
Expected response	After step 1:	The IUT shall receive the TST_FRM_10_RESP_0-12 as 12 data bytes regardless of the L_FI_DLC value.
	After step 2:	The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE and shall report to the UT.
Remark	---	

Table 22 — TC – 2.CTC_2.6 – L_FI_DLC ≠ 1111_2 and frame data verification 2 if DLC is 1101_2 or 1110_2

CTC-DLL-TC	Value of L_FI_DLC
2.CTC_2.6-1	1101_2
2.CTC_2.6-2	1110_2

7.3.7 2.CTC_2.7 – L_FI_DLC = 1111_2/L_FI_DLCext ≥ 0 and frame data verification

Table 23 specifies the CTC that verifies the 2.CTC_2.7 – L_FI_DLC = 1111_2/L_FI_DLCext ≥ 0 and frame data verification.

Table 23 — 2.CTC_2.7 – L_FI_DLC = 1111_2/L_FI_DLCext ≥ 0 and frame data verification

Item	Content
CTC # – Title	2.CTC_2.7 – L_FI_DLC = 1111_2/L_FI_DLCext ≥ 0 and frame data verification
Purpose	This CTC verifies that the DLCext field of the frame of L_FI_DLC ≥ 1111_2 complies with the CXPI specification. This CTC is applicable only to an IUT, which supports the L_FI_DLC = 1111_2.
Reference	ISO 20794-4:2020: — REQ 0.5 SIP – PDU, protocol data unit; — REQ 0.6 SIP – Length, length of PDU; — REQ 2.9 DLL – L_FI configuration; — REQ 2.11 DLL – L_FI_DLCext (data length code extension); — REQ 2.30 DLL – Function models – DLL – Transmission logic.
Prerequisite	The test system set-up shall be in accordance with Figure 2. This test is applicable only to IUTs which support frames of L_FI_DLC = 1111_2.

Table 23 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to default configurations (see 6.6.3) and in addition support TST_FRM_01_REQ_PID and TST_FRM_12_RESP_LONG_0-255. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to transmit TST_FRM_01_REQ_PID and TST_FRM_12_RESP_LONG_0-255 changing the L_FI_DLCext with all possible data length values.
Iteration	REPEAT step 1 up to the maximum value of the L_FI_DLCext which is supported by the IUT; UT in IUT shall change the L_FI_DLCext value according to the data length of the test frame; REPEAT END.
Expected response	After step 1: The IUT shall transmit the TST_FRM_12_RESP_LONG_0-255 which complies with ISO 20794-4:2020, 8.4.3.3. The IUT shall transmit the L_FI_DLC value = 1111_2. The IUT shall transmit the L_FI_DLCext value which meets the data length size. The LT shall receive the L_FI_DLC value = 1111_2. The LT shall receive the L_FI_DLCext value which meets the data length size and shall report to the UT.
Remark	---

7.3.8 2.CTC_2.8 – Given CRC of frame with L_FI_DLC ≠ 1111_2

Table 24 specifies the CTC that verifies the 2.CTC_2.8 – Given CRC of frame with L_FI_DLC ≠ 1111_2.

Table 24 — 2.CTC_2.8 – Given CRC of frame with L_FI_DLC ≠ 1111_2

Item	Content
CTC # – Title	2.CTC_2.8 – Given CRC of frame with L_FI_DLC ≠ 1111_2
Purpose	This CTC verifies that the CRC field for the L_FI_DLC ≠ 1111_2 frame complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 2.16 DLL – L_CRC field determination; — REQ 2.17 DLL – CRC8 calculation; — REQ 2.30 DLL – Function models – DLL – Transmission logic.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to default configurations (see 6.6.3) and in addition support TST_FRM_01_REQ_PID and TST_FRM_10_RESP_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12 changing the L_FI_DLC.

Table 24 *(continued)*

Item	Content
Iteration	REPEAT step 1 up to the maximum value of the L_FI_DLC which is supported by the IUT; UT in IUT shall change the L_FI_DLC value according to the data length of the test frame; REPEAT END.
Expected response	After step 1: The IUT shall transmit the CRC8 calculation which complies with ISO 20794-4:2020, 8.4.5.2. The LT shall receive the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12 changing the L_FI_DLC value with all possible data length values and shall report to the UT.
Remark	---

7.3.9 2.CTC_2.9 – Given CRC of frame with L_FI_DLC = 1111_2/L_FI_DLCext ≥ 0

Table 25 specifies the CTC that verifies the 2.CTC_2.9 – Given CRC of frame with L_FI_DLC = 1111_2/L_FI_DLCext ≥ 0.

Table 25 — 2.CTC_2.9 – Given CRC of frame with L_FI_DLC = 1111_2/L_FI_DLCext ≥ 0

Item	Content
CTC # – Title	2.CTC_2.9 – Given CRC of frame with L_FI_DLC = 1111_2/L_FI_DLCext ≥ 0
Purpose	This CTC verifies that the CRC field for the L_FI_DLCext ≥ 0 frame complies with the CXPI specification. This CTC is applicable only to an IUT, which supports L_FI_DLC = 1111_2.
Reference	ISO 20794-4:2020: — REQ 2.16 DLL – L_CRC field determination; — REQ 2.18 DLL – CRC16 calculation; — REQ 2.30 DLL – Function models – DLL – Transmission logic.
Prerequisite	The test system set-up shall be in accordance with Figure 2. This test is applicable only to IUTs which support frame of L_FI_DLC = 1111_2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to default configurations (see 6.6.3) and in addition support TST_FRM_01_REQ_PID and TST_FRM_12_RESP_LONG_0-255. The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to transmit the TST_FRM_01_REQ_PID and the TST_FRM_12_RESP_LONG_0-255 changing the the L_FI_DLCext value.
Iteration	REPEAT step 1 up to the maximum value of the L_FI_DLCext which is supported by the IUT; UT in IUT shall change the L_FI_DLCext value according to the data length of the test frame; REPEAT END.
Expected response	After step 1: The IUT shall transmit the CRC16 calculation which complies with ISO 20794-4:2020, 8.4.5.3. The LT shall receive the TST_FRM_01_REQ_PID and the TST_FRM_12_RESP_LONG_0-255 changing the L_FI_DLCext value with all possible data length values and shall report to the UT.
Remark	---

7.3.10 2.CTC_2.10 – Frame transmission completion

Table 26 specifies the CTC that verifies the 2.CTC_2.10 – Frame transmission completion.

Table 26 — 2.CTC_2.10 – Frame transmission completion

Item	Content
CTC # – Title	2.CTC_2.10 – Frame transmission completion
Purpose	This CTC verifies that the completion of transmission frame complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 2.28 DLL – Completing condition of frame.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet2 configurations (see 6.6.5) and in addition support TST_FRM_01_REQ_PID, TST_FRM_10_RESP_0-12, TST_FRM_03_REQ_PID_UNKNOWN, TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12. 2. The LT shall transmit the TST_FRM_03_REQ_PID_UNKNOWN after recognizing IFS of the bit length specified in Table 27 (from the end of transmitted the CRC of the TST_FRM_10_RESP_0-12). 3. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT.
Iteration	Steps are executed for each test case specified in Table 27; REPEAT step 1 to 3, 2 times; The LT shall set the IFS as specified in Table 27; REPEAT END.
Expected response	See Table 27.
Remark	---

Table 27 — TC – 2.CTC_2.10 – Frame transmission completion

CTC-DLL-TC	IFS	Judgement criteria
2.CTC_2.10-1	11 bit	After step 6: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE and shall report to the UT.
2.CTC_2.10-2	9 bit	After Step 6: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE and shall report to the UT.

7.3.11 2.CTC_2.11 – Frame reception completion

Table 28 specifies the CTC that verifies the 2.CTC_2.11 – Frame reception completion.

Table 28 — 2.CTC_2.11 – Frame reception completion

Item	Content
CTC # – Title	2.CTC_2.11 – Frame reception completion
Purpose	This CTC verifies that the completion of reception frame complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 2.28 DLL – Completing condition of frame.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet2 configurations (see 6.6.5) and in addition support TST_FRM_01_REQ_PID, TST_FRM_10_RESP_0-12, TST_FRM_03_REQ_PID_UNKNOWN, TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12. 2. The LT shall transmit the TST_FRM_03_REQ_PID_UNKNOWN after recognizing an IFS of the bit length specified in Table 29 (from the end of transmitted CRC of the TST_FRM_10_RESP_0-12). 3. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT.
Iteration	Steps are executed for each test case specified in Table 29; REPEAT step 1 to step 3, 2 times; The LT shall set the IFS as specified in Table 29; REPEAT END.
Expected response	See Table 29.
Remark	---

Table 29 — TC – 2.CTC_2.11 – Frame reception completion

CTC-DLL-TC	IFS	Judgement criteria	
CTC_2.11-1	11 bit	After step 2:	The IUT shall receive the same data as transmitted by the test system.
		After step 3:	The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE.
			The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE and shall report to the UT.
2.CTC_2.11-2	9 bit	After step 2:	The IUT shall discard the received frame.
		After step 3:	The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE.
			The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE and shall report to the UT.

7.4 CTP – Network access

7.4.1 2.CTC_3.1 – Arbitration function 1 (arbitration by using carrier sense)

Table 30 specifies the CTC that verifies the 2.CTC_3.1 – Arbitration function 1 (arbitration by using carrier sense).

Table 30 — 2.CTC_3.1 – Arbitration function 1 (arbitration by using carrier sense)

Item	Content
CTC # – Title	2.CTC_3.1 – Arbitration function 1 (arbitration by using carrier sense)
Purpose	This CTC verifies that the arbitration function of the L_PTYPE field or the L_PID field complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 2.29 DLL – Byte arbitration.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_Unknown configurations (see 6.6.7) and in addition support TST_FRM_01_REQ_PID, TST_FRM_03_REQ_PID_UNKNOWN and TST_FRM_13_RESP_UNKOWN_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The LT shall transmit the consecutive TST_FRM_03_REQ_PID_UNKNOWN and the TST_FRM_13_RESP_UNKOWN_0-12 with an 18-bit IFS interval. 2. The UT shall control the IUT to transmit the TST_FRM_01_REQ_PID.
Iteration	Not applicable
Expected response	After step 2: The IUT shall not transmit the TST_FRM_01_REQ_PID. The LT shall not receive the TST_FRM_01_REQ_PID. The IUT shall not corrupt the TST_FRM_03_REQ_PID_UNKNOWN and the TST_FRM_13_RESP_UNKOWN_0-12.
Remark	---

7.4.2 2.CTC_3.2 – Arbitration function 2 (IUT loses arbitration and transitions into receiving state)

Table 31 specifies the CTC that verifies the 2.CTC_3.2 – Arbitration function 2 (IUT loses arbitration and transitions into receiving state).

Table 31 — 2.CTC_3.2 – Arbitration function 2 (IUT loses arbitration and transitions into receiving state)

Item	Content
CTC # – Title	2.CTC_3.2 – Arbitration function 2 (IUT loses arbitration and transitions into receiving state)
Purpose	This CTC verifies that the IUT as receiving node complies with the CXPI specification after losing arbitration.
Reference	ISO 20794-4:2020, REQ 2.29 DLL – Byte arbitration.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_Arbit configurations (see 6.6.6) and in addition support TST_FRM_01_REQ_PID, TST_FRM_10_RESP_0-12, TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to transmit the TST_FRM_01_REQ_PID. 2. The LT shall transmit the TST_FRM_01_REQ_PID with the higher priority than IUT and the TST_FRM_10_RESP_0-12 to generate arbitration lost on IUT. 3. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT.
Iteration	Not applicable
Expected response	After step 2: The IUT shall receive the same data that the LT transmits. After step 3: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE and shall report to the UT.
Remark	---

7.5 CTP – Error detection

7.5.1 2.CTC_4.1 – Byte error

Table 32 specifies the CTC that verifies the 2.CTC_4.1 – Byte error.

Table 32 — 2.CTC_4.1 – Byte error

Item	Content
CTC # – Title	2.CTC_4.1 – Byte error
Purpose	This CTC verifies that the detection function of the byte error complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 0.11 SIP – Result, result; — REQ 2.32 DLL – Byte error (Err_DLL_Byte).
Prerequisite	The test system set-up shall be in accordance with Figure 2.

Table 32 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.4) and in addition support TST_FRM_00_REQ_PTYPE, TST_FRM_01_REQ_PID and TST_FRM_10_RESP_0-12, TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to transmit the TST_FRM_00_REQ_PTYPE (see remark 1), the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12. 2. The LT shall invert any bit in the TST_FRM_00_REQ_PTYPE (see remark 1), the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12 transmitted by the IUT according to Table 33 (refer to remark 2). 3. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT.
Iteration	Steps are executed for each test case specified in Table 33; REPEAT step 1 to step 3, 21 times; The LT shall set the IBS as specified in Table 33; REPEAT END.
Expected response	After step 2: The IUT shall stop the transmission from the point where a byte error is detected for each test case. The LT shall not receive the TST_FRM_10_RESP_0-12. After step 3: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE and shall report to the UT.
Remark	1. The TST_FRM_00_REQ_PTYPE is only applicable to the IUTs which support polling method. 2. Step 2 shall be executed with step 1 cooperated with the IUT.

Table 33 — TC – 2.CTC_4.1 – Byte error

CTC-DLL-TC	Response field coverage	Bit position to be inverted[a]	IBS length
2.CTC_4.1-1	L_PID field or L_PTYPE field	Start bit	---
2.CTC_4.1-2	L_PID field or L_PTYPE field	Stop bit	---
2.CTC_4.1-3	IBS between L_PID field and L_FI_field	Bit 1	≥1 bit
2.CTC_4.1-4	L_FI_field	Start bit	---
2.CTC_4.1-5	L_FI_field	Bit 2	---
2.CTC_4.1-6	L_FI_field	Bit 4	---
2.CTC_4.1-7	L_FI_field	Bit 6	---
2.CTC_4.1-8	L_FI_field	Stop bit	---
2.CTC_4.1-9	IBS between L_FI_field and L_DATA 1	Bit 1	≥1 bit
2.CTC_4.1-10	L_DATA 1	Start bit	---
2.CTC_4.1-11	L_DATA 1	Bit 0	---
2.CTC_4.1-12	L_DATA 1	Bit 1	---
2.CTC_4.1-13	L_DATA 1	Bit 2	---

[a] The IBS and IFS bit counting is started at the stop bit of the previous data byte.

[b] The DATA N is the last data byte of the TST_FRM_10_RESP_0-12.

Table 33 *(continued)*

CTC-DLL-TC	Response field coverage	Bit position to be inverted[a]	IBS length
2.CTC_4.1-14	L_DATA 1	Bit 3	---
2.CTC_4.1-15	L_DATA 1	Bit 4	---
2.CTC_4.1-16	L_DATA 1	Bit 5	---
2.CTC_4.1-17	L_DATA 1	Bit 6	---
2.CTC_4.1-18	L_DATA 1	Bit 7	---
2.CTC_4.1-19	L_DATA 1	Stop bit	---
2.CTC_4.1-20	IBS between L_DATA N[b] and L_CRC	Bit 1	≥1 bit
2.CTC_4.1-21	L_CRC	Any bit (bit 0 to bit 7)	≥1 bit

[a] The IBS and IFS bit counting is started at the stop bit of the previous data byte.

[b] The DATA N is the last data byte of the TST_FRM_10_RESP_0-12.

7.5.2 2.CTC_4.2 – CRC error

Table 34 specifies the CTC that verifies the 2.CTC_4.2 – CRC error.

Table 34 — 2.CTC_4.2 – CRC error

Item	Content
CTC # – Title	2.CTC_4.2 – CRC error
Purpose	This CTC verifies that the detection function of the CRC error complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 0.11 SIP – Result, result; — REQ 2.31 DLL – Function models – DLL – Reception logic; — REQ 2.33 DLL – CRC error (Err_DLL_CRC).
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.4) and in addition support TST_FRM_01_REQ_PID, TST_FRM_10_RESP_0-12, TST_FRM_12_RESP_LONG_0-255, TST_FRM_05_REQ_PID_ERRBIT, and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	Supported function: L_FI_DLC ≠ 1111_2 1. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12 with inverted bits in the CRC field. 2. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT. Supported function: L_FI_DLC = 1111_2 3. The LT shall transmit the TST_FRM_01_REQ_PID and TST_FRM_12_RESP_LONG_0-255 with inverted bits in the CRC field. 4. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT. Supported function: L_FI_DLC ≠ 1111_2 and L_FI_DLC = 1111_2

Table 34 *(continued)*

Item	Content
	1. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12 with inverted bits in the CRC field. 2. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT. 3. The LT shall transmit the TST_FRM_01_REQ_PID and TST_FRM_12_RESP_LONG_0-255 with inverted bits in the CRC field. 4. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT.
Iteration	Not applicable
Expected response	After step 1: The IUT shall discard the received data. After step 2: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE and shall report to the UT. After step 3: The IUT shall discard the received data. After step 4: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE and shall report to the UT.
Remark	---

7.5.3 2.CTC_4.3 – Parity error of the L_PID field without the error bit

Table 35 specifies the CTC that verifies the 2.CTC_4.3 – Parity error of the L_PID field without the error bit.

Table 35 — 2.CTC_4.3 – Parity error of the L_PID field without the error bit

Item	Content
CTC # – Title	2.CTC_4.3 – Parity error of the L_PID field without the error bit
Purpose	This CTC verifies that the detection function of the parity error of the L_PID field complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 0.11 SIP – Result, result; — REQ 2.31 DLL – Function models – DLL – Reception logic; — REQ 2.34 DLL – Parity error (Err_DLL_Parity).
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to default configurations (see 6.6.4) and in addition support TST_FRM_01_REQ_PID and TST_FRM_10_RESP_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The LT shall transmit the TST_FRM_01_REQ_PID with the inverted parity bit of the L_PID field for the IUT to transmit the TST_FRM_10_RESP_0-12.
Iteration	Not applicable
Expected response	After step 1: The IUT shall not transmit the TST_FRM_10_RESP_0-12. The LT shall not receive the TST_FRM_10_RESP_0-12.
Remark	---

7.5.4 2.CTC_4.4 – Parity error of the L_PID field with the error bit

Table 36 specifies the CTC that verifies the 2.CTC_4.4 – Parity error of the L_PID field with the error bit.

Table 36 — 2.CTC_4.4 – Parity error of the L_PID field with the error bit

Item	Content
CTC # – Title	2.CTC_4.4 – Parity error of the L_PID field with the error bit
Purpose	This CTC verifies that the detection function of the parity error of the L_PID field complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 0.11 SIP – Result, result; — REQ 2.31 DLL – Function models – DLL – Reception logic; — REQ 2.34 DLL – Parity error (Err_DLL_Parity).
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.4) and in addition support TST_FRM_01_REQ_PID, TST_FRM_10_RESP_0-12, TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The LT shall transmit the TST_FRM_01_REQ_PID with the inverted parity bit of the L_PID filed. 2. The LT shall transmit the TST_FRM_10_RESP_0-12. 3. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT.
Iteration	Not applicable
Expected response	After step 2: The IUT shall discard the received data of the TST_FRM_10_RESP_0-12. After step 3: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE and shall report to the UT.
Remark	---

7.5.5 2.CTC_4.5 – Parity error of the L_PTYPE field without the error bit

Table 37 specifies the CTC that verifies the 2.CTC_4.5 – Parity error of the L_PTYPE field without the error bit.

Table 37 — 2.CTC_4.5 – Parity error of the L_PTYPE field without the error bit

Item	Content
CTC # – Title	2.CTC_4.5 – Parity error of the L_PTYPE field without the error bit
Purpose	This CTC verifies that the detection function of the Parity error of the L_PTYPE field complies with the CXPI specification.
Reference	ISO 20794-4:2020:

Table 37 *(continued)*

Item	Content
	— REQ 0.11 SIP – Result, result; — REQ 2.31 DLL – Function models – DLL – Reception logic; — REQ 2.34 DLL – Parity error (Err_DLL_Parity).
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a slave node. — The IUT shall be configured to L_ default configurations (see 6.6.4) and in addition support TST_FRM_00_REQ_PTYPE and TST_FRM_01_REQ_PID. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to transmit the TST_FRM_01_REQ_PID. 2. The LT shall transmit the TST_FRM_00_REQ_PTYPE with the inverted parity bit.
Iteration	Not applicable
Expected response	After step 2: The IUT shall not transmit the TST_FRM_01_REQ_PID. The LT shall not receive the TST_FRM_01_REQ_PID.
Remark	---

7.5.6 2.CTC_4.6 – Parity error of the L_PTYPE field with the error bit

Table 40 specifies the CTC that verifies the 2.CTC_4.6 – Parity error of the L_PTYPE field with the error bit.

Table 38 — 2.CTC_4.6 – Parity error of the L_PTYPE field with the error bit

Item	Content
CTC # – Title	2.CTC_4.6 – Parity error of the L_PTYPE field with the error bit
Purpose	This CTC verifies that the detection function of the Parity error of the L_PTYPE field complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 0.11 SIP – Result, result; — REQ 2.31 DLL – Function models – DLL – Reception logic; — REQ 2.34 DLL – Parity error (Err_DLL_Parity).
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.4) and in addition support TST_FRM_00_REQ_PTYPE, TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The LT shall transmit the TST_FRM_00_REQ_PTYPE with the inverted parity bit. 2. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT.
Iteration	Not applicable

Table 38 *(continued)*

Item	Content	
Expected response	After step 2:	The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE.
Remark	---	

7.5.7 2.CTC_4.7 – Data length code error with L_FI_DLC ≠ 1111_2

Table 39 specifies the CTC that verifies the 2.CTC_4.7 – Data length code error with L_FI_DLC ≠ 1111_2.

Table 39 — 2.CTC_4.7 – Data length code error with L_FI_DLC ≠ 1111_2

Item	Content
CTC # – Title	2.CTC_4.7 – Data length code error with L_FI_DLC ≠ 1111_2
Purpose	This CTC verifies that the detection function of the data length code error complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 0.11 SIP – Result, result; — REQ 2.31 DLL – Function models – DLL – Reception logic; — REQ 2.35 DLL – Data length code error (Err_DLL_DLC).
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.4) and in addition support TST_FRM_10_RESP_0-12, TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	Condition 1: In case that the data field size is longer than the size specified by the L_FI_DLC value. 1. The LT shall transmit the TST_FRM_10_RESP_0-12 which consists of the data field longer than the size specified by the L_FI_DLC value. At the time of setting up the CRC, the CRC value shall be calculated based on the correct data field range specified by the L_FI_DLC value (i.e. the CRC error would not occur if the data field is sent with the correct size). 2. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT. Condition 2: In case that the data field size is shorter than the size specified by the L_FI_DLC value. 3. The LT shall transmit the TST_FRM_10_RESP_0-12 which consists of the data field shorter than the size specified by the L_FI_DLC value; 4. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT.
Iteration	Not applicable
Expected response	After step 1: The IUT shall not receive the TST_FRM_10_RESP_0-12. The LT shall transmit the TST_FRM_10_RESP_0-12. After step 2: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE and shall report to the UT.

Table 39 *(continued)*

Item	Content
	After step 3: The IUT shall not receive the TST_FRM_10_RESP_0-12. The LT shall transmit the TST_FRM_10_RESP_0-12. After step 4: The IUT shall transmit theTST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE and shall report to the UT.
Remark	---

7.5.8 2.CTC_4.8 – Data length error with L_FI_DLC = 1111_2/L_FI_DLCext ≥ 0

Table 40 specifies the CTC that verifies the 2.CTC_4.8 – Data length error with L_FI_DLC = 1111_2/L_FI_DLCext ≥ 0.

Table 40 — 2.CTC_4.8 – Data length error with L_FI_DLC = 1111_2/L_FI_DLCext ≥ 0

Item	Content
CTC # – Title	2.CTC_4.8 – Data length error with L_FI_DLC = 1111_2/L_FI_DLCext ≥ 0
Purpose	This CTC verifies that the detection function of the data length code error complies with the CXPI specification. This test is applicable only to an IUT, which supports the L_FI_DLC = 1111_2.
Reference	ISO 20794-4:2020: — REQ 0.11 SIP – Result, result; — REQ 2.31 DLL – Function models – DLL – Reception logic; — REQ 2.35 DLL – Data length code error (Err_DLL_DLC).
Prerequisite	The test system set-up shall be in accordance with Figure 2. This test is applicable only to IUTs which support L_FI_DLC = 1111_2 frame.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.4) and in addition support TST_FRM_01_REQ_PID, TST_FRM_12_RESP_LONG_0-255, TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	Condition 1: In case that the data field size is longer than the size specified by the L_FI_DLCext value. 1. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_12_RESP_LONG_0-255 which consist of the data field longer than the size specified by the extension DLC value. At the time of setting up the CRC, the CRC value shall be calculated based on the correct data field range specified by the extension DLC value (i.e. the CRC error would not occur if the data field is sent with the correct size). 2. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT. Condition 2: In case that the data field size is shorter than the size specified by the L_FI_DLCext value. 3. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_12_RESP_LONG_0-255 which consist of the data field shorter than the size specified by the extension L_FI_DLC value. 4. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT.

Table 40 *(continued)*

Item	Content
	Condition 3: In case that the response is only the 1st byte of the frame information (L_FI). 5. The LT shall transmit the TST_FRM_01_REQ_PID and the frame information (L_FI) of TST_FRM_12_RESP_LONG_0-255. 6. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT.
Iteration	Not applicable.
Expected response	After step 1: The IUT shall not receive the TST_FRM_12_RESP_LONG_0-255. The LT shall transmit the TST_FRM_12_RESP_LONG_0-255. After step 2: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE and shall report to the UT. After step 3: The IUT shall not receive the TST_FRM_12_RESP_LONG_0-255. The LT shall transmit the TST_FRM_12_RESP_LONG_0-255. After step 4: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE and shall report to the UT. After step 5: The IUT shall not receive the TST_FRM_12_RESP_LONG_0-255. The LT shall transmit the TST_FRM_12_RESP_LONG_0-255. After Step 6: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE and shall report to the UT.
Remark	---

7.5.9 2.CTC_4.9 – Data length code error L_FI_DLC ≠ 1111_2 and if DLC is 1101_2 or 1110_2 (Ftype = DiagNodeCfg)

Table 41 specifies the CTC that verifies the 2.CTC_4.9 – Data length code error L_FI_DLC ≠ 1111_2 and if DLC is 1101_2 or 1110_2 (Ftype = DiagNodeCfg).

Table 41 — 2.CTC_4.9 – Data length code error L_FI_DLC ≠ 1111_2 and if DLC is 1101_2 or 1110_2 (Ftype = DiagNodeCfg)

Item	Content
CTC # – Title	2.CTC_4.9 – Data length code error L_FI_DLC ≠ 1111_2 and if DLC is 1101_2 or 1110_2 (Ftype = DiagNodeCfg)
Purpose	This CTC verifies that the detection function of the data length code error complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 0.11 SIP – Result, result; — REQ 2.36 DLL – Data length code error (Err_DLL_DLC) – L_FI_DLC = [D_{16} to E_{16}]; — REQ 2.37 DLL – Data length code error (Err_DLL_DLC) – L_FI_DLC = [D_{16} to E_{16}] L_Result = Err_DLL_DLC.
Prerequisite	The test system set-up shall be in accordance with Figure 2.

Table 41 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.4) and in addition support TST_FRM_01_REQ_PID and TST_FRM_10_RESP_0-12 (only L_Length = $0C_{16}$). — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_10_RESP_0-12 changing the DLC value as specified in Table 42.
Iteration	Steps are executed for each test case specified in Table 42; REPEAT step 1, 2 times; The LT shall set the L_FI_DLC value as specified in Table 42; REPEAT END.
Expected response	After step 1: The IUT shall not transmit any messages. The LT shall not receive any messages.
Remark	---

Table 42 — TC –2.CTC_4.9 – Data length code error L_FI_DLC ≠ 1111_2 and if DLC is 1101_2 or 1110_2 (Ftype = DiagNodeCfg)

CTC-DLL-TC	Value of L_FI_DLC
2.CTC_4.7-1	1101_2
2.CTC_4.7-2	1110_2

7.5.10 2.CTC_4.10 – Data length code error L_FI_DLC = 1111_2/L_FI_DLCext ≤ 12 (Ftype = DiagNodeCfg)

Table 43 specifies the CTC that verifies the 2.CTC_4.10 – Data length code error L_FI_DLC = 1111_2/L_FI_DLCext ≤ 12 (Ftype = DiagNodeCfg).

Table 43 — 2.CTC_4.10 – Data length code error L_FI_DLC = 1111_2/L_FI_DLCext ≤ 12 (Ftype = DiagNodeCfg)

Item	Content
CTC # – Title	2.CTC_4.10 – Data length code error L_FI_DLC = 1111_2/L_FI_DLCext ≤ 12 (Ftype = DiagNodeCfg)
Purpose	This CTC verifies that the detection function of the data length code error complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 0.11 SIP – Result, result; — REQ 2.38 DLL – Data length code error (Err_DLL_DLC) – L_FI_DLCext = [0_{16} to C_{16}]; — REQ 2.39 DLL – Data length code error (Err_DLL_DLC) – L_FI_DLCext = [0_{16} to C_{16}] – L_Result = Err_DLL_DLCext.
Prerequisite	The test system set-up shall be in accordance with Figure 2.

Table 43 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.4) and in addition support TST_FRM_01_REQ_PID, and TST_FRM_13_RESP_LONG_0-255. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_13_RESP_LONG_0-255 (L_FI_DLCext ≤ 12).
Iteration	Not applicable.
Expected response	After step 1: The IUT shall not transmit any messages. The LT shall not receive any messages.
Remark	---

7.5.11 2.CTC_4.11 – Framing error in receiving node

Table 44 specifies the CTC that verifies the 2.CTC_4.11 – Framing error in receiving node.

Table 44 — 2.CTC_4.11 – Framing error in receiving node

Item	Content
CTC # – Title	2.CTC_4.11 – Framing error in receiving node
Purpose	This CTC verifies that the behaviour of the IUT as the receiving node complies with the CXPI specification when it detects the framing error.
Reference	ISO 20794-4:2020: — REQ 0.11 SIP – Result, result; — REQ 2.40 DLL – Framing error (Err_DLL_Framing).
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.4) and in addition support TST_FRM_01_REQ_PID, TST_FRM_10_RESP_0-12, TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The LT shall transmit the TST_FRM_01_REQ_PID or the TST_FRM_10_RESP_0-12 including the framing error. 2. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT.
Iteration	Not applicable
Expected response	After step 1: The IUT shall stop the reception processing and discard the frame which is received. After step 2: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE and shall report to the UT.
Remark	---

7.5.12 2.CTC_4.12 – Framing error in transmitting node

Table 45 specifies the CTC that verifies the 2.CTC_4.12 – Framing error in transmitting node.

Table 45 — 2.CTC_4.12 – Framing error in transmitting node

Item	Content
CTC # – Title	2.CTC_4.12 – Framing error in transmitting node
Purpose	This CTC verifies that the behaviour of the IUT as the transmitting node complies with the CXPI specification when it detects the framing error.
Reference	ISO 20794-4:2020: — REQ 0.11 SIP – Result, result; — REQ 2.40 DLL – Framing error (Err_DLL_Framing).
Prerequisite	The test system set-up shall be in accordance with Figure 2
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.4) and in addition support TST_FRM_01_REQ_PID, TST_FRM_10_RESP_0-12, TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT shall transmit the TST_FRM_01_REQ_PID or the TST_FRM_10_RESP_0-12. 2. The LT shall apply the forced inversion to a stop bit at any data byte of the data field (refer to remark 1). 3. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT.
Iteration	Not applicable
Expected response	After step 2: The IUT shall stop the transmission processing immediately and waits until the IFS is detected (IUT does not transmit). The LT shall not receive the TST_FRM_10_RESP_0-12. After step 3: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = TRUE and shall report to the UT.
Remark	1. Step 2 shall be run with step 1 cooperated with the IUT.

7.5.13 2.CTC_4.13 – Ignore error (no support of L_FI_DLC = 1111_2)

Table 46 specifies the CTC that verifies the 2.CTC_4.13 – Ignore error (no support of L_FI_DLC = 1111_2).

Table 46 — 2.CTC_4.13 – Ignore error (no support of L_FI_DLC = 1111_2)

Item	Content
CTC # – Title	2.CTC_4.13 – Ignore error (no support of L_FI_DLC = 1111_2)
Purpose	This CTC verifies that the behaviour of the IUT at the time of receiving the frame of L_FI_DLC = 1111_2 complies with the CXPI specification. This CTC is applicable only to an IUT, which not supports the L_FI_DLC = 1111_2.
Reference	ISO 20794-4:2020, REQ 2.41 DLL – Exception handling for L_FI_DLC = '1111_2' detection.
Prerequisite	The test system set-up shall be in accordance with Figure 2.

Table 46 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a master node or a slave node. — The IUT shall be configured to L_ErrDet1 configurations (see 6.6.4) and in addition support TST_FRM_01_REQ_PID, TST_FRM_12_RESP_LONG_0-255 (only L_Length = FF_{16}), TST_FRM_05_REQ_PID_ERRBIT and TST_FRM_16_RESP_ERRBIT_0-12. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	Condition of generated error: the CRC 1. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_12_RESP_LONG_0-255 including the CRC error. 2. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT. Condition of generated error: data length code 3. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_12_RESP_LONG_0-255 including the data length code error. 4. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT. Condition of generated error: Framing 5. The LT shall transmit the TST_FRM_01_REQ_PID and the TST_FRM_12_RESP_LONG_0-255 including the framing error. 6. The LT shall transmit the TST_FRM_05_REQ_PID_ERRBIT.
Iteration	Not applicable
Expected response	After step 2: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE and shall report to the UT. After step 4: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE and shall report to the UT. After Step 6: The IUT shall transmit the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE. The LT shall receive the TST_FRM_16_RESP_ERRBIT_0-12 with the error bit = FALSE and shall report to the UT.
Remark	---

8 Physical layer conformance test plan (PMA – PS separate type)

8.1 CTP – Operational conditions and calibration

8.1.1 Initial configuration

This test describes the initial configuration for each test. The test specific requirements are defined in each test case.

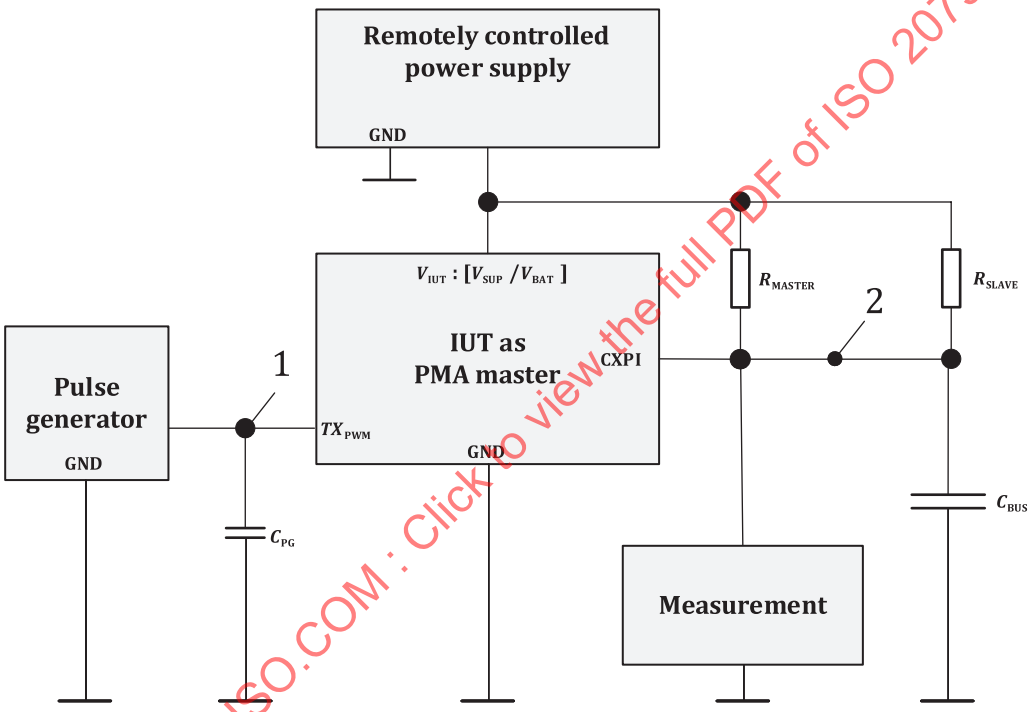
The initial state of electrical input/output is described in Table 47.

Table 47 — Initial state of electrical input/output

IUT set-up	
Operational conditions	**Definition**
CXPI network loads	Defined for each test
IUT state	Initial state
V_{BAT}, V_{SUP}, V_{IUT}	Defined for each test
Failure	No failure
GND shift	0 V
Bit rate	Maximum bit rate in the specification of the IUT

8.1.2 1.CTC_1.1 – Clock transmission 1

The test system set-up for this test is shown in Figure 13.



Key

1	TX_{PWM}
2	CXPI network
Components	
C_{PG}	capacitance
C_{BUS}	total bus capacitance
R_{MASTER}	master node resistor
R_{SLAVE}	slave node resistor

Figure 13 — Test system – Clock transmission 1 test set-up

Table 48 specifies the CTC that verifies the 1.CTC_1.1 – Clock transmission 1.

Table 48 — 1.CTC_1.1 – Clock transmission 1

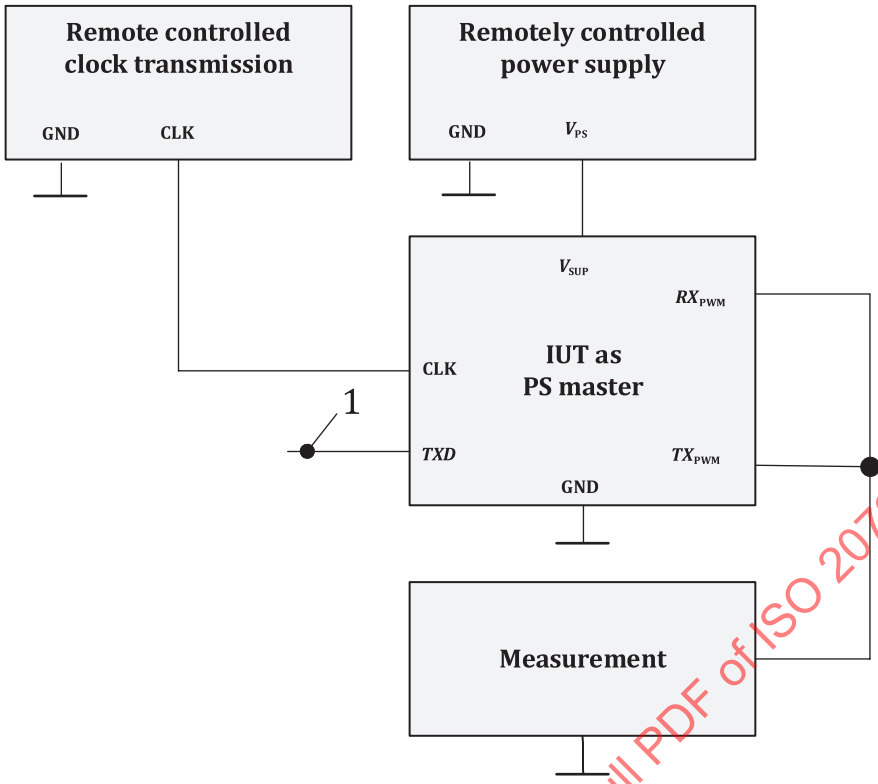
Item	Content
CTC # – Title	1.CTC_1.1 – Clock transmission 1
Purpose	This CTC verifies that the clock output function of the IUT complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 1.14 PHY – PMA AC parameters $D_{tx\_1\_lo\_dom}$, $D_{tx\_1\_lo\_rec}$; — REQ 1.14 PHY – PMA AC parameters $t_{tx\_pwm\_slope\_clk}$.
Prerequisite	The test system set-up shall be in accordance with Figure 13.
Set-up	— The IUT shall be configured as a master node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to the L_PwrMng1 (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}]: see Table 49. — R_{MASTER}: see Table 49. — R_{SLAVE}: see Table 49. — C_{BUS}: see Table 49. — V_{Dom_TS}: see Table 49. — V_{Rec_TS}/$V_{Pull\text{-}up}$: see Table 49. — *TX*: C_{PG} = 20 pF (±5 %).
Step	1. The IUT shall be powered. 2. The pulse generator shall provide a duty cycle in the range of 0,11 to 0,45 to the TX_{PWM} terminal.
Iteration	Step 1 and step 2 shall be executed for each test case specified in Table 49.
Expected response	After step 2: The IUT shall transmit a clock onto the CXPI network. The measurement shall observe the PWM waveform and shall measure $D_{tx\_1\_lo\_dom} \geq 0{,}11$, $D_{tx\_1\_lo\_rec} \leq 0{,}45$ and $t_{tx\_pwm\_slope\_clk} \leq 8$ µs.
Remark	---

Table 49 — 1.CTC_1.1 – Clock transmission 1

CTC-EPL-TC	V_{IUT}: [V_{SUP}/ V_{BAT}]	V_{Dom_TS}	V_{Rec_TS}/ $V_{Pull\text{-}up}$	R_{MASTER}	R_{SLAVE}	C_{BUS}
CTC_1.1-1	8 V	0 V	8 V	1 kΩ (±0,1 %)	30 kΩ (±0,1 %)	4 nF (±1 %)
CTC_1.1-2	13 V	0 V	13 V			
CTC_1.1-3	18 V	0 V	18 V			

8.1.3 1.CTC_1.2 – Clock transmission 2

The test system set-up for this test is shown in Figure 14.



Key

1 Fixed to HI level

Figure 14 — Test system – Clock transmission 2 test set-up

Table 50 specifies the CTC that verifies the 1.CTC_1.2 – Clock transmission 2.

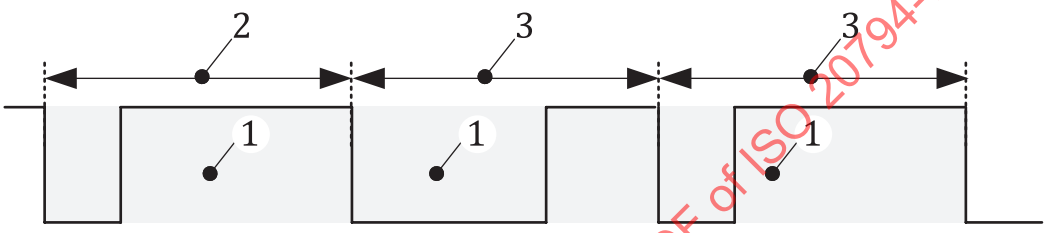
Table 50 — 1.CTC_1.2 – Clock transmission 2

Item	Content
CTC # – Title	1.CTC_1.2 – Clock transmission 2
Purpose	This CTC verifies that the clock output function of the IUT complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 1.1 PHY – PS bit rate; — REQ 1.5 PHY – PS clock generation; — REQ 1.6 PHY – PS clock generation - Transmitter jitter Δt_{bit_cont}.
Prerequisite	The test system set-up shall be in accordance with Figure 14.
Set-up	— The IUT shall be configured as a master node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to the L_PwrMng1 (see 6.7). — V_{IUT} [V_{SUP}]: 13 V. — The *TXD* of the IUT shall be set to HI level. — V_{CC} shall be set to 5 V or 3,3 V depending on the SUT.

Table 50 *(continued)*

Item	Content
Step	1. The IUT shall be powered. 2. The remote-controlled clock transmission shall provide a duty cycle of 0,5 to the CLK terminal.
Iteration	Not applicable
Expected response	After step 2: The IUT shall transmit the PWM waveform at the TX_{PWM} terminal. The measurement shall observe the PWM waveform and shall measure Δt_{bit_cont} within ±0,5 % of the nominal bit time.
Remark	---

The PWM waveform Δt_{bit_cont} of the clock transmission for this test is shown in Figure 15.



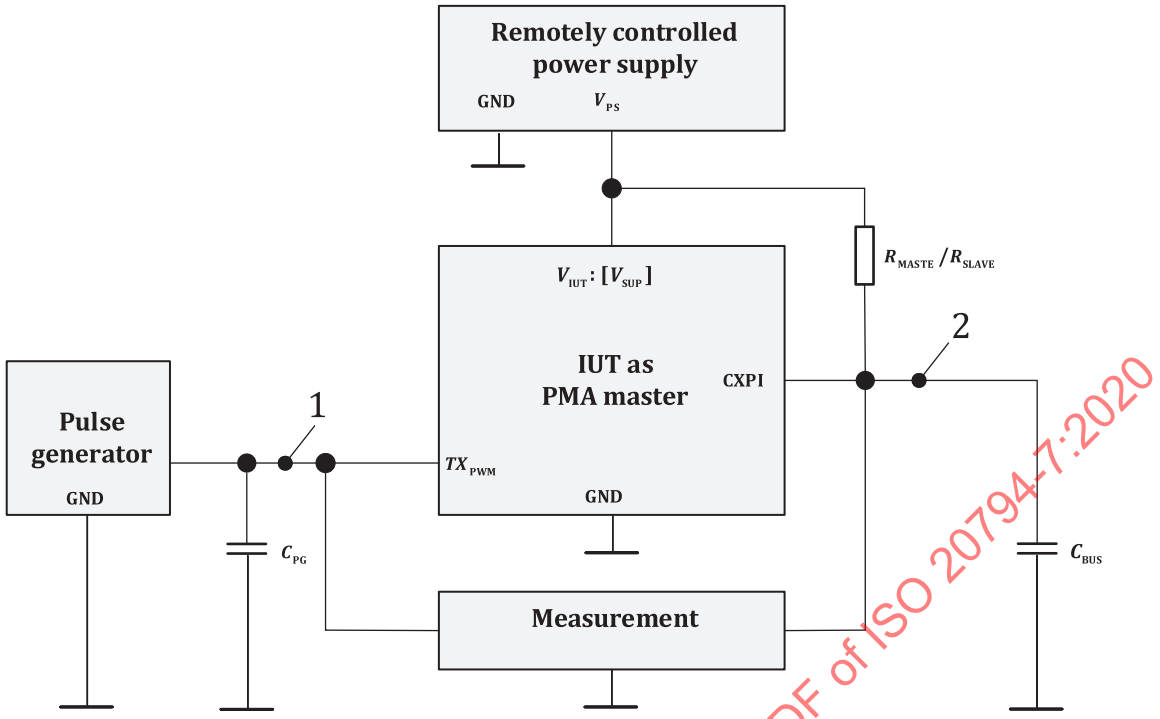
Key

1 TX_{PWM}
2 t_{bit_ref} (bit width of reference bit rate)
3 $t_{bit\_ref} \times (1 + \Delta t_{bit\_cont})$

Figure 15 — Test system – Clock transmission 2 PWM waveform

8.1.4 1.CTC_1.3 – Clock transmission 3

The test system set-up for this test is shown in Figure 16.



Key

1	TX_{PWM}
2	CXPI network
Components	
C_{PG}	capacitance
C_{BUS}	total bus capacitance
R_{MASTER}	master node resistor
R_{SLAVE}	slave node resistor

Figure 16 — Test system – Clock transmission 3 test set-up

Table 51 specifies the CTC that verifies the 1.CTC_1.3 – Clock transmission 3.

Table 51 — 1.CTC_1.3 – Clock transmission 3

Item	Content
CTC # – Title	1.CTC_1.3 – Clock transmission 3
Purpose	This CTC verifies that the clock output function of the IUT complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 1.14 PHY – PMA AC parameters Δt_{bit_driver}.
Prerequisite	The test system set-up shall be in accordance with Figure 16.
Set-up	— The IUT shall be configured as a master node (1.CTC_1.3-1 to 1.CTC_1.3-3). — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to the L_PwrMng1 (see 6.7). — V_{IUT}: [V_{SUP}]: see Table 52. — *TXD*: C_{PG} = 20 pF (±5 %).
Step	1. The IUT shall be powered. 2. The pulse generator shall provide a duty cycle in the range of 0,11 to 0,45 to the TX_{PWM} terminal.

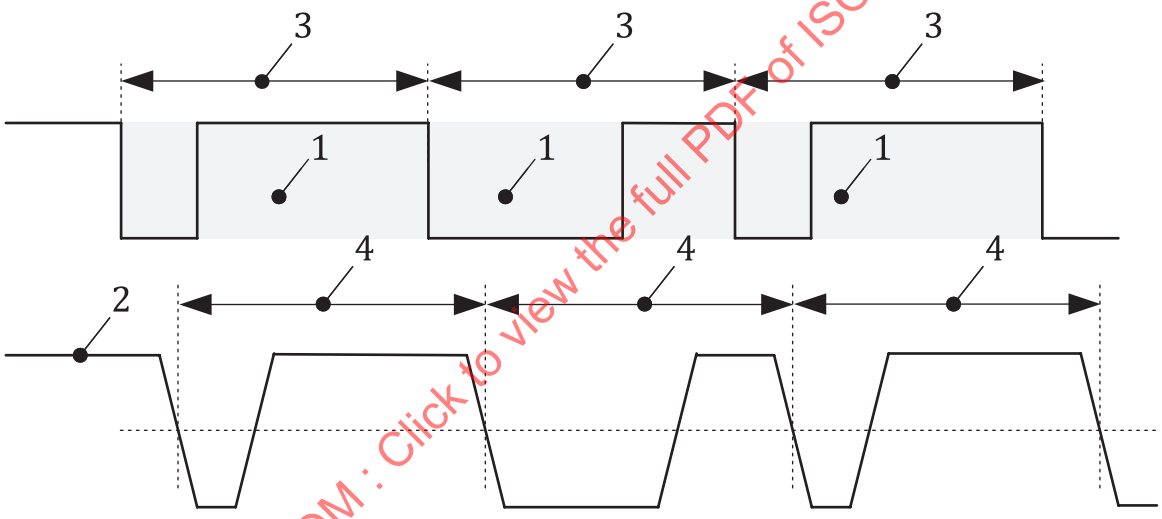
Table 51 *(continued)*

Item	Content	
Iteration	Step 1 and step 2 shall be executed for each test case specified in Table 52.	
Expected response	After step 2:	The IUT shall transmit the CXPI waveform onto the CXPI network. The measurement shall observe the PWM waveform and shall measure Δt_{bit_driver} within ±0,5 % of the nominal bit time.
Remark	---	

Table 52 — TC – 1.CTC_1.3 – Clock transmission 3

CTC-EPL-TC	V_{IUT}: [V_{SUP}]	R_{MASTER}	R_{SLAVE}	C_{BUS}
1.CTC_1.3-1	7 V	1 kΩ (±0,1 %)	30 kΩ (±0,1 %)	4 nF (±1 %)
1.CTC_1.3-2	13 V			
1.CTC_1.3-3	18 V			

The PWM waveform Δt_{bit_driver} of the clock transmission for this test is shown in Figure 17.



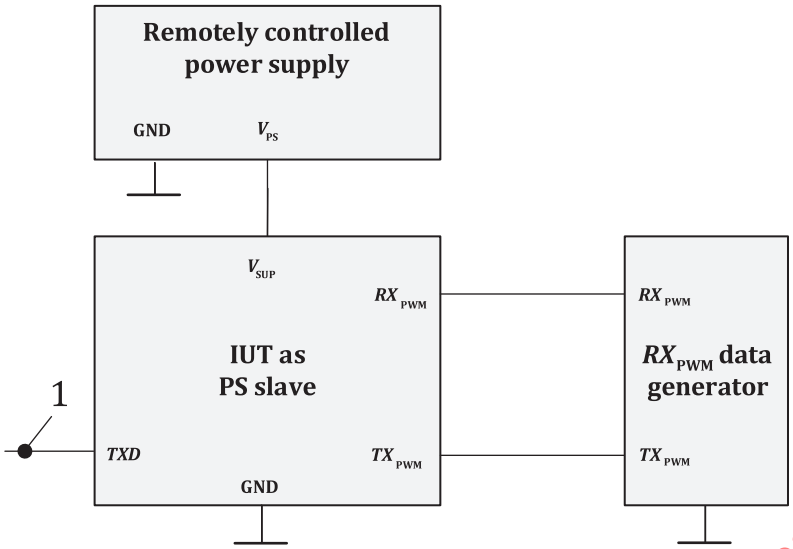
Key

1 TX_{PWM}
2 CXPI network
3 t_{bit_ref} (bit width of reference bit rate)
4 $t_{bit\_ref} \times (1 + \Delta t_{bit\_driver})$

Figure 17 — Test system – Clock transmission 3 PWM waveform

8.1.5 1.CTC_1.4 – Detection of clock existence

The test system set-up for this test is shown in Figure 18.



Key

1 Fixed to HI level

Figure 18 — Test system – Detection of clock existence test set-up

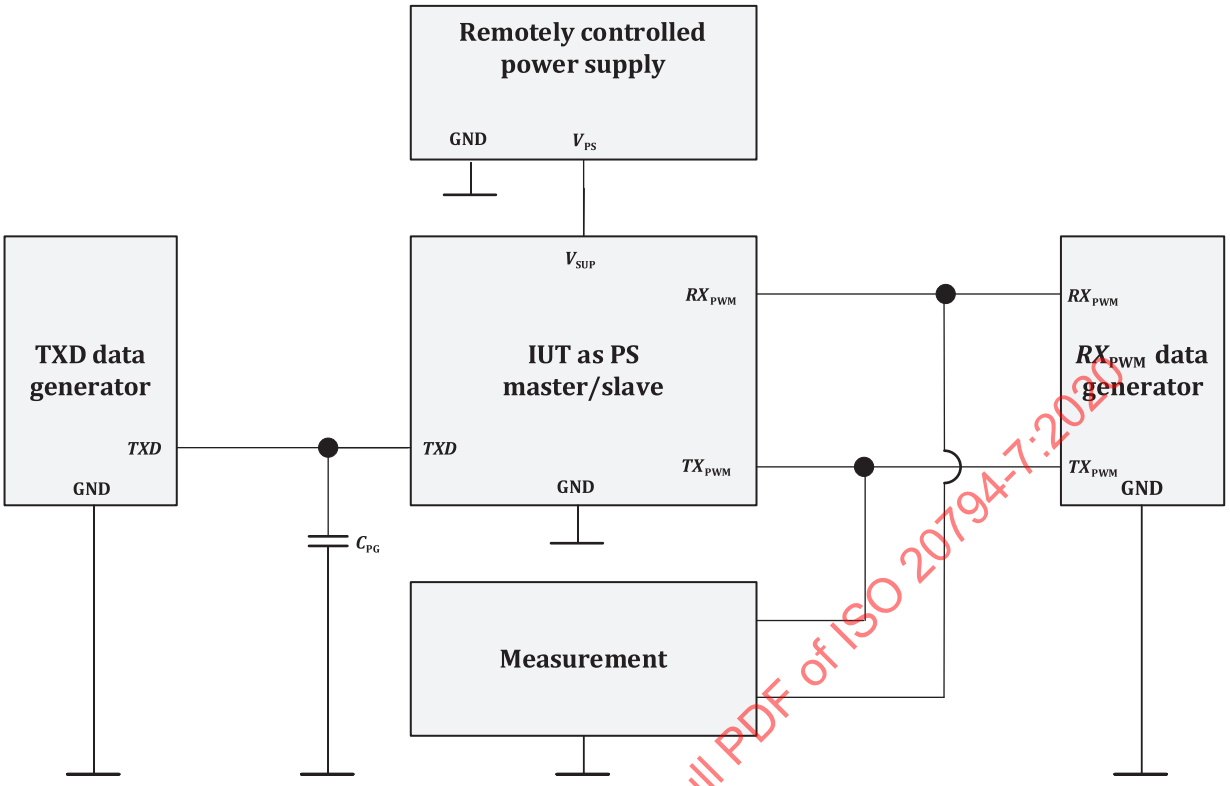
Table 53 specifies the CTC that verifies the 1.CTC_1.4 – Detection of clock existence.

Table 53 — 1.CTC_1.4 – Detection of clock existence

Item	Content
CTC # – Title	1.CTC_1.4 – Detection of clock existence
Purpose	This CTC verifies that the detection function of the clock existence.
Reference	ISO 20794-4:2020: — REQ 0.7 SIP – ev_wakeup_ind, event wake-up indication (optional); — REQ 1.9 PHY – PS detection of clock existence.
Prerequisite	The test system set-up shall be in accordance with Figure 18.
Set-up	— The IUT shall be configured as a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to the L_PwrMng1 (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}]: 13 V.
Step	1. The IUT shall be powered. 2. The RX_{PWM} data generator shall start transmitting the clock as a waveform.
Iteration	Not applicable
Expected response	After step 2: The IUT shall notify the clock existence.
Remark	---

8.1.6 1.CTC_1.5 – Arbitration function (stop transmission by arbitration)

The test system set-up for this test is shown in Figure 19.



Component

C_{PG} capacitance

Figure 19 — Test system – Arbitration function (stop transmission by arbitration) test set-up

Table 54 specifies the CTC that verifies the 1.CTC_1.5 – Arbitration function (stop transmission by arbitration).

Table 54 — 1.CTC_1.5 – Arbitration function (stop transmission by arbitration)

Item	Content
CTC # – Title	1.CTC_1.5 – Arbitration function (stop transmission by arbitration)
Purpose	This CTC verifies that the arbitration of the bit collisions complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 1.10 PHY – PS bit-wise collision resolution.
Prerequisite	The test system set-up shall be in accordance with Figure 19.
Set-up	— The IUT shall be configured as a master node or a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}]: 13 V. — *TXD*: C_{PG} = 20 pF (±5 %).
Step	1. The *TXD* data generator shall transmit a logical value of 1or a logical value of 0. 2. The RX_{PWM} data generator shall collide any bit in logical value '0' of RX_{PWM} with any bit in logical value '1' of RX_{PWM} excluding the parity bit.
Iteration	Not applicable

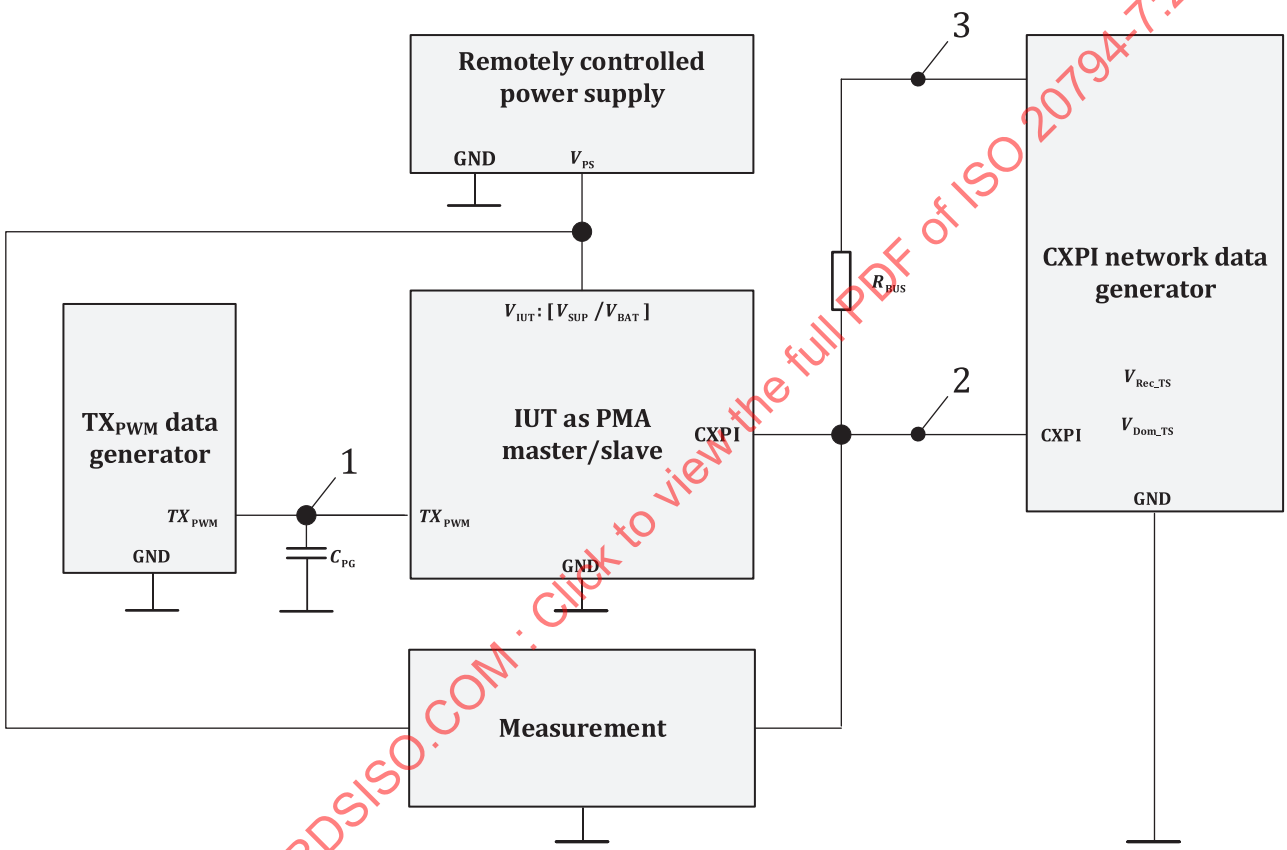
Table 54 *(continued)*

Item	Content	
Expected response	After step 2:	The IUT shall stop the transmission of logical value '0' after any bit in logical value '0' of RX_{PWM} collision. The measurement shall observe stop the transmission on the TX_{PWM}.
Remark	---	

8.1.7 1.CTC_1.6 – Operating voltage range

Verify valid operational voltage with transmission and reception.

The test system set-up for this test is shown in Figure 20.



Key

1	TX_{PWM}
2	CXPI network
3	$V_{Pull\text{-}up}$
Components	
C_{PG}	capacitance
R_{BUS}	total CXPI network resistance

Figure 20 — Test system – Operating voltage range test set-up

Table 55 specifies the CTC that verifies the 1.CTC_1.6 – Operating voltage range.

Table 55 — 1.CTC_1.6 – Operating voltage range

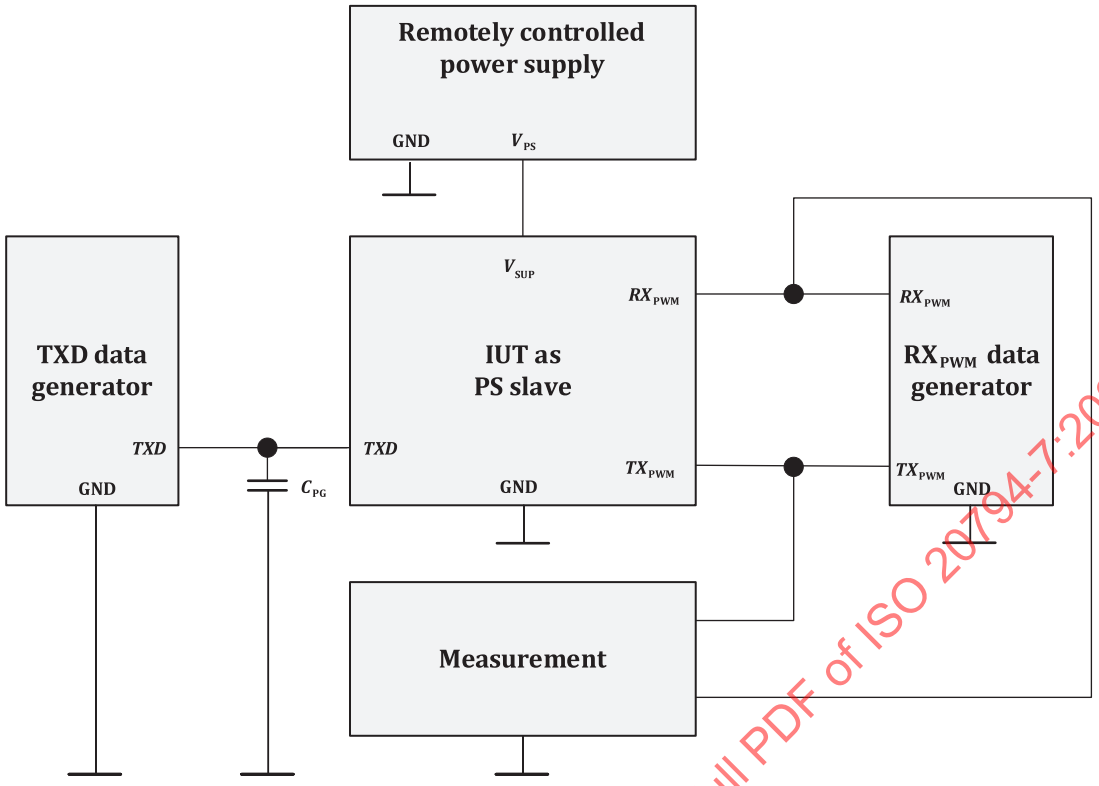
Item	Content
CTC # – Title	1.CTC_1.6 – Operating voltage range
Purpose	This CTC verifies that the IUT operates correctly in the valid supply voltage ranges.
Reference	ISO 20794-4:2020: — REQ 1.13 PHY – PMA electrical parameters V_{BAT}; — REQ 1.13 PHY – PMA electrical parameters V_{SUP}.
Prerequisite	The test system set-up shall be in accordance with Figure 20.
Set-up	— The IUT shall be configured as a master node (1.CTC_1.6-1 or 1.CTC_1.6-2) or a slave node (1.CTC_1.6-3 or 1.CTC_1.6-4). — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to the L_PwrMng1 (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}]: see Table 56. — R_{BUS}: see Table 56. — V_{Dom_TS}: 0 V. — V_{Rec_TS}/$V_{Pull\text{-}up}$: see Table 56. — TX_{PWM}: C_{PG} = 20 pF (±5 %).
Step	1. The remotely controlled power supply shall be set on the V_{BAT}/V_{SUP} as specified in Table 56. 2. The TX_{PWM} data generator shall transmit the PWM waveform.
Iteration	Step 1 and step 2 shall be executed for each test case specified in Table 56.
Expected response	During step 2: The IUT shall transmit and receive the PWM waveform continuously under all conditions. The measurement shall observe the PWM waveform on the TX_{PWM}.
Remark	---

Table 56 — TC – 1.CTC_1.6 – Operating voltage range

CTC-EPL-TC	V_{IUT} range: [V_{SUP} range/V_{BAT} range]	V_{Rec_TS}/$V_{Pull\text{-}up}$	Signal ramp	R_{BUS}
CTC_1.6-1	[7,0 V to 18 V]/[8,0 V to 18 V]	[8,0 V to 18 V]	0,1 V/s	30 kΩ (±0,1 %)
CTC_1.6-2	[18 V to 7,0 V]/[18 V to 8,0 V]	[18 V to 8,0 V]	0,1 V/s	30 kΩ (±0,1 %)
CTC_1.6-3	[7,0 V to 18 V]/[8,0 V to 18 V]	[8,0 V to 18 V]	0,1 V/s	1 kΩ (±0,1 %)
CTC_1.6-4	[18 V to 7,0 V]/[18 V to 8,0 V]	[18 V to 8,0 V]	0,1 V/s	1 kΩ (±0,1 %)

8.1.8 1.CTC_1.7 – Bit synchronisation

The test system set-up for this test is shown in Figure 21.



Component

C_{PG} capacitance

Figure 21 — Test system – Bit synchronisation test set-up

Table 57 specifies the CTC that verifies the 1.CTC_1.7 – Bit synchronisation.

Table 57 — 1.CTC_1.7 – Bit synchronisation

Item	Content
CTC # – Title	1.CTC_1.7 – Bit synchronisation
Purpose	This CTC verifies that the IUT perform communication processing by synchronizing with the clock.
Reference	ISO 20794-4:2020, REQ 1.8 PHY – PS node clock synchronisation and bit synchronization.
Prerequisite	The test system set-up shall be in accordance with Figure 21.
Set-up	— The IUT shall be configured as a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}]: 13 V. — *TXD*: C_{PG} = 20 pF (±5 %).
Step	1. The RX_{PWM} data generator shall transmit the clock as a waveform. 2. The *TXD* data generator shall transmit a logical value of 1or a logical value of 0.
Iteration	Not applicable
Expected response	After step 2: The IUT shall transmit the PWM waveform in synchronization with the falling edge of clock. The measurement shall observe the PWM waveform on the TX_{PWM}.
Remark	---

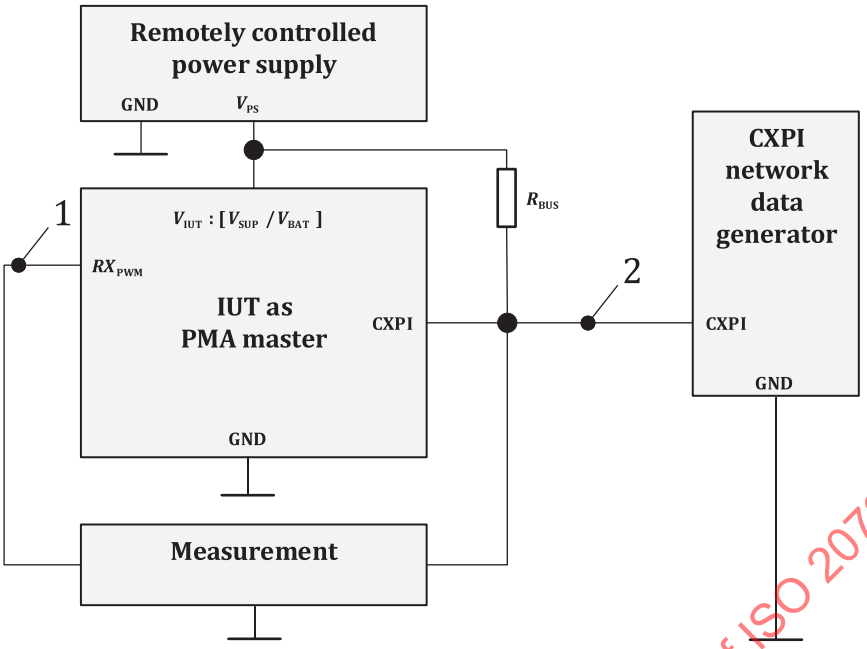
8.2 CTP – Wake-up pulse

8.2.1 General

This subclause describes the behaviour of the IUT when it receives the wake-up pulse. All tests described in this section are applicable only to the IUTs which support ISO 20794-2.

8.2.2 1.CTC_2.1 – Wake-up pulse reception 1, IUT as master node

The test system set-up for this test is shown in Figure 22.



Key

1	RX_{PWM}
2	CXPI network
Component	
R_{BUS}	total CXPI network resistance

Figure 22 — Test system – Wake-up pulse reception 1, IUT as master node test set-up

Table 58 specifies the CTC that verifies the 1.CTC_2.1 – Wake-up pulse reception 1, IUT as master node.

Table 58 — 1.CTC_2.1 – Wake-up pulse reception 1, IUT as master node

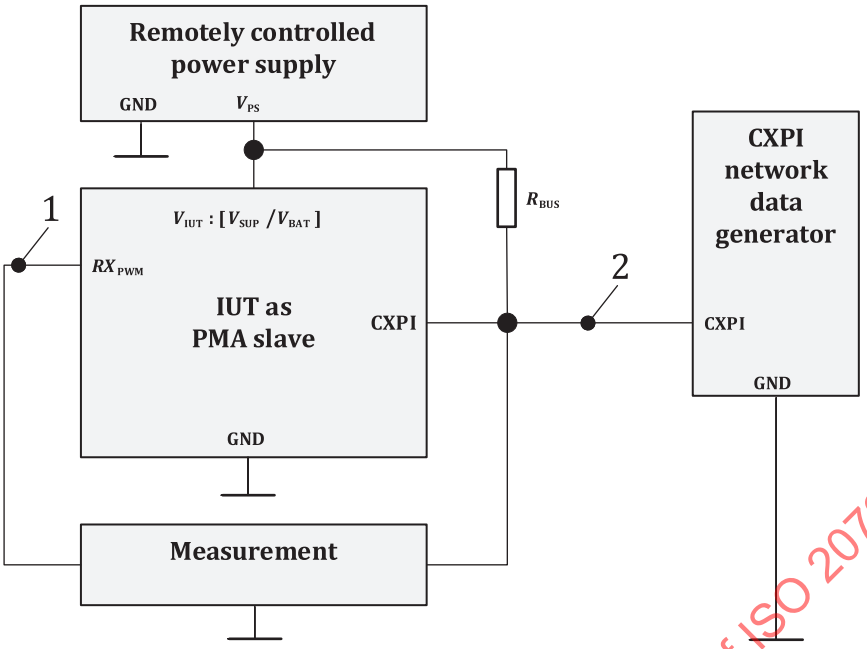
Item	Content
CTC # – Title	1.CTC_2.1 – Wake-up pulse reception 1, IUT as master node
Purpose	This CTC verifies that the behaviour of the IUT when receiving the wake-up pulse complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 0.7 SIP – `ev_wakeup_ind`, event wake-up indication (optional); — REQ 1.16 PHY – PMA wake-up pulse and dominant pulse filter time $t_{rx\_wakeup\_clk}$.
Prerequisite	The test system set-up shall be in accordance with Figure 22. This CTC is only applicable to a master node.
Set-up	— The IUT shall be configured as a master node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to the L_PwrMng2 (see 6.7).
Step	1. The CXPI network data generator shall transmit the wake-up pulse as specified in Table 59.
Iteration	Step 1 shall be executed for each test case as specified in Table 59.
Expected response	After step 1: See Table 59.
Remark	---

Table 59 — TC – 1.CTC_2.1 – Wake-up pulse reception 1, IUT as master

CTC-EPL-TC	Wake-up pulse parameter	Value	Judgement criteria
1.CTC_2.1-1	t_{tx_wakeup}	400 µs	After step 1: The IUT shall notify the wake-up reception.
	$t_{tx\_wakeup\_space}$	5 ms	
1.CTC_2.1-2	t_{tx_wakeup}	2 500 µs	
	$t_{tx\_wakeup\_space}$	5 ms	
1.CTC_2.1-3	t_{tx_wakeup}	400 µs	
	$t_{tx\_wakeup\_space}$	10 ms	
1.CTC_2.1-4	t_{tx_wakeup}	2 500 µs	
	$t_{tx\_wakeup\_space}$	10 ms	
1.CTC_2.1-5	t_{tx_wakeup}	29 µs	After step 1 The IUT shall not wake-up.

8.2.3 1.CTC_2.2 – Wake-up pulse reception 2, IUT as slave node

The test system set-up for this test is shown in Figure 23.



Key

1	RX_{PWM}
2	CXPI network
Component	
R_{BUS}	total CXPI network resistance

Figure 23 — Test system – Wake-up pulse reception 2, IUT as slave node test set-up

Table 60 specifies the CTC that verifies the 1.CTC_2.2 – Wake-up pulse reception 2, IUT as slave node.

Table 60 — 1.CTC_2.2 – Wake-up pulse reception 2, IUT as slave node

Item	Content
CTC # – Title	1.CTC_2.2 – Wake-up pulse reception 2, IUT as slave node
Purpose	This CTC verifies that the behaviour of the IUT when receiving the wake-up pulse (i.e. clock) complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 0.7 SIP – ev_wakeup_ind, event wake-up indication (optional); — REQ 1.16 PHY – PMA wake-up pulse and dominant pulse filter time t_{rx_wakeup}; — REQ 1.16 PHY – PMA wake-up pulse and dominant pulse filter time $t_{rx\_wakeup\_space}$.
Prerequisite	The test system set-up shall be in accordance with Figure 23. This test is only applicable to a slave node.
Set-up	— The IUT shall be configured as a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to the L_PwrMng2 (see 6.7).
Step	1. The CXPI network data generator shall transmit the clock waveform as specified in Table 61.
Iteration	Step 1 shall be executed for each test case specified in Table 61.
Expected response	After step 1: See Table 61.

Table 60 *(continued)*

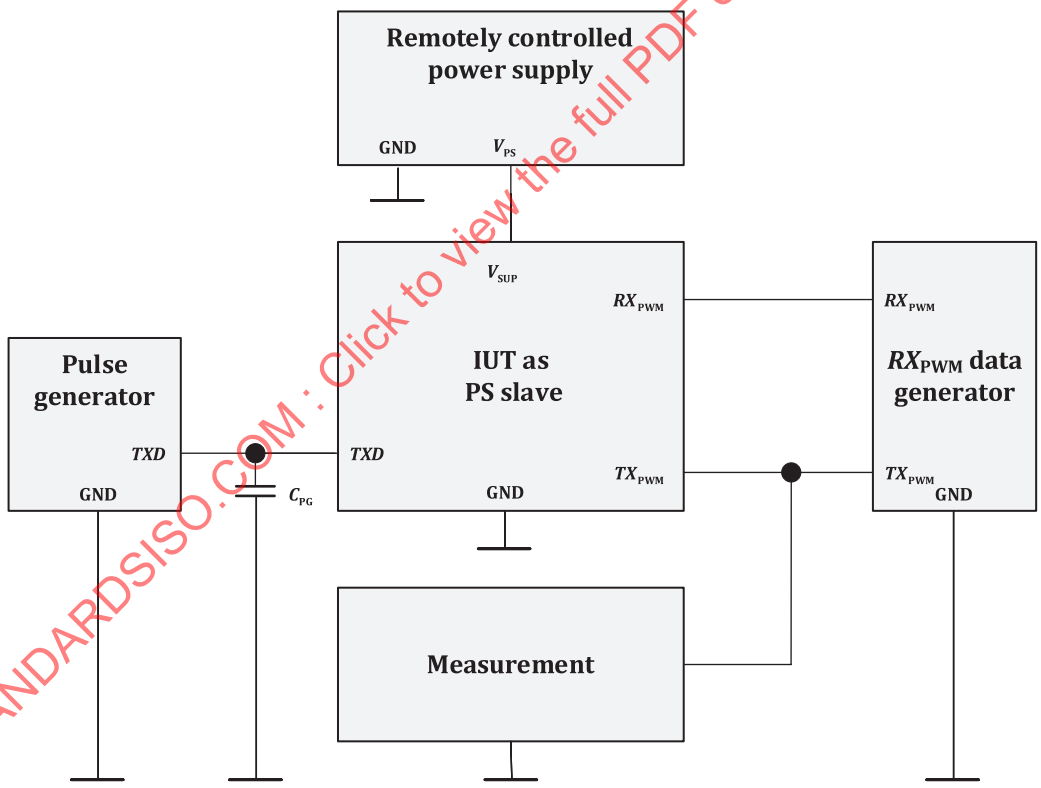
Item	Content
Remark	---

Table 61 — TC – 1.CTC_2.2 – Wake-up pulse reception 2, IUT as slave

CTC-EPL-TC	Conditions		Expected response
1.CTC_2.2-1	$D_{tx\_1\_lo\_dom}$ = 0,11	Inclination rate of waveform <5 V/µs;	After step 1: The IUT shall notify the wake-up reception.
1.CTC_2.2-2	$D_{tx\_1\_lo\_rec}$ = 0,45		
1.CTC_2.2-3	The CXPI network data generator shall transmit the dominant level with 0,4 µs duration in 1 t_{bit} interval.		After step 1: The IUT shall not wake-up.
1.CTC_2.2-4	The CXPI network data generator shall transmit the dominant level with 0.25 t_{bit} duration in 61 ms interval.		After step 1: The IUT shall not wake-up.

8.2.4 1.CTC_2.3 – Wake-up pulse transmission

The test system set-up for this test is shown in Figure 24.



Component

C_{PG} capacitance

Figure 24 — Test system – Wake-up pulse transmission test set-up

Table 62 specifies the CTC that verifies the 1.CTC_2.3 – Wake-up pulse transmission.

Table 62 — 1.CTC_2.3 – Wake-up pulse transmission

Item	Content
CTC # – Title	1.CTC_2.3 – Wake-up pulse transmission
Purpose	This CTC verifies that the function of the transmission of the wake-up pulse by a slave node complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 0.8 SIP – cmd_wakeup_req, command wake-up request; — REQ 1.12 PHY – PS node transmission of wake-up pulse t_{tx_wakeup}; — REQ 1.12 PHY – PS node transmission of wake-up pulse $t_{tx\_wakeup\_space}$.
Prerequisite	The test system set-up shall be in accordance with Figure 24.
Set-up	— The IUT shall be configured as a slave node (1.CTC_2.3-1 or 1.CTC_2.3-2). — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to the L_PwrMng2 (see 6.7). — *TXD*: C_{PG} = 20 pF (±5 %).
Step	1. The pulse generator shall transmit the wake-up pulse as specified in Table 63.
Iteration	Step 1 shall be executed for each test case specified in Table 63.
Expected response	After step 1: See Table 63.
Remark	---

Table 63 — TC – 1.CTC_2.3 – Wake-up pulse transmission

CTC-EPL-TC	Definition	Judgement criteria	
1.CTC_2.3-1	The RX_{PWM} data generator shall receive first dominant pulse which the IUT shall transmit and shall transmit the clock after 4 ms elapsed.	After step 1:	The IUT shall transmit the wake-up pulse which meets 400 µs ≤ t_{tx_wakeup} ≤ 2 500 µs. The measurement shall observe the wake-up pulse which meets 400 µs ≤ t_{tx_wakeup} ≤ 2 500 µs. The start point of the measurement shall be the fall edge of the waveform and the end point of the measurement shall be the rise edge of the waveform. The IUT shall not transmit the second dominant pulse. The measurement shall not observe the second dominant pulse.
1.CTC_2.3-2	The RX_{PWM} data generator shall receive second dominant pulse which the IUT shall transmit and shall transmit the clock within 59 ms.	After step 1:	The IUT shall transmit the wake-up pulse, which meets 400 µs ≤ t_{tx_wakeup} ≤ 2 500 µs and 5 ms ≤ $t_{tx\_wakeup\_space}$ ≤ 10 ms. The measurement shall observe the wake-up pulse, which meets 400 µs ≤ t_{tx_wakeup} ≤ 2 500 µs and 5 ms ≤ $t_{tx\_wakeup\_space}$ ≤ 10 ms. The start point of the measurement shall be the fall edge of the waveform and the end point of the measurement shall be the rise edge of the waveform.

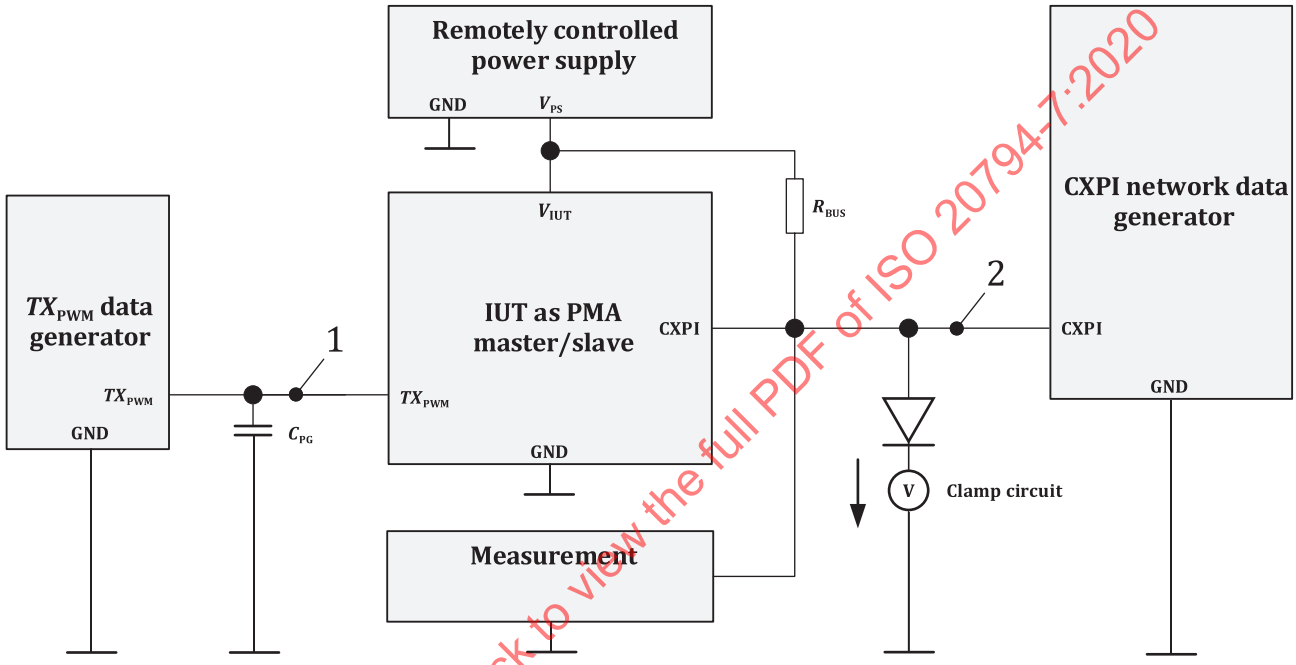
8.3 CTP – Voltage and duty cycle thresholds

8.3.1 General

All CTCs specified in 8.3 verify the threshold voltages and threshold duty cycle of the IUT are implemented correctly within the specified operating supply voltage range.

8.3.2 Voltage threshold test set-up

This set-up of the test system is shown in Figure 25.



Key

1	TX_{PWM}
2	CXPI network
Components	
C_{PG}	capacitance
R_{BUS}	total CXPI network resistance

Figure 25 — Test system – Voltage threshold test 1 set-up

8.3.3 1.CTC_3.1 – Voltage threshold test 1

Table 64 specifies the CTC that verifies the 1.CTC_3.1 – Voltage threshold test 1.

Table 64 — 1.CTC_3.1 – Voltage threshold test 1

Item	Content
CTC # – Title	1.CTC_3.1 – Voltage threshold test 1
Purpose	This CTC verifies that the IUT operates the correct voltage threshold.
Reference	ISO 20794-4:2020: — REQ 1.13 PHY – PMA electrical parameters V_{BUSdom}; — REQ 1.13 PHY – PMA electrical parameters V_{BUSrec}.
Prerequisite	The test system set-up shall be in accordance with Figure 25.

Table 64 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a master node (1.CTC_3.1-1 to 1.CTC_3.1-3) or a slave node (1.CTC_3.1-4 to 1.CTC_3.1-6). — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}]: see Table 65. — V_{Dom_TS}: see Table 65. — V_{Rec_TS}/$V_{Pull\text{-}up}$: see Table 65. — R_{BUS}: see Table 65. — TX_{PWM}: C_{PG} = 20 pF (±5 %).
Step	1. The TX_{PWM} data generator shall control the IUT to transmit and receive the PWM waveform (refer to remark 1).
Iteration	Step 1 is executed for each test case specified in Table 65.
Expected response	After step 1: The IUT shall transmit and receive the PWM waveform.
Remark	1. The clamp circuit in Figure 25 is used as necessary to realize the recessive voltage of V_{Rec_TS}.

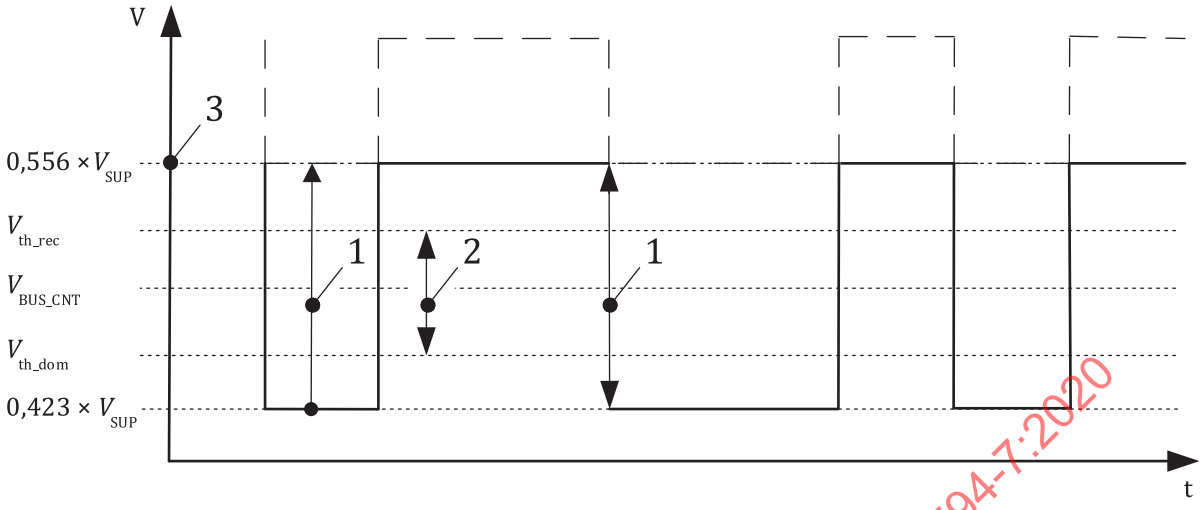
The V_{SUP} shall be calculated from the V_{BAT} by knowing the characteristic of the IUT.

Table 65 — TC – 1.CTC_3.1 – Voltage threshold test 1

CTC-EPL-TC	V_{IUT}: [V_{SUP}]	V_{Dom_TS}/$V_{Rec\text{-}TS}$	Expected communication result	R_{BUS}
1.CTC_3.1-1	7 V	V_{Rec_TS} = 0,556 × V_{SUP} = 3,892 V/ V_{Dom_TS} = 0,423 × V_{SUP} = 2,961 V	Successful	30 kΩ (±0,1 %)
1.CTC_3.1-2	13 V	V_{Rec_TS} = 0,556 × V_{SUP} = 7,228 V/ V_{Dom_TS} = 0,423 × V_{SUP} = 5,499 V	Successful	
1.CTC_3.1-3	18 V	V_{Rec_TS} = 0,556 × V_{SUP} = 10,008 V/ V_{Dom_TS} = 0,423 × V_{SUP} = 7,614 V	Successful	
1.CTC_3.1-4	7 V	V_{Rec_TS} = 0,556 × V_{SUP} = 3,892 V/ V_{Dom_TS} = 0,423 × V_{SUP} = 2,961 V	Successful	1 kΩ (±0,1 %)
1.CTC_3.1-5	13 V	V_{Rec_TS} = 0,556 × V_{SUP} = 7,228 V/ V_{Dom_TS} = 0,423 × V_{SUP} = 5,499 V	Successful	
1.CTC_3.1-6	18 V	V_{Rec_TS} = 0,556 × V_{SUP} = 10,008 V/ V_{Dom_TS} = 0,423 × V_{SUP} = 7,614 V	Successful	

8.3.4 1.CTC_3.2 – Voltage threshold (V_{Dom_TS} up) test 2

Figure 26 shows an example of test (V_{Dom_TS} up) – Voltage threshold test 2.

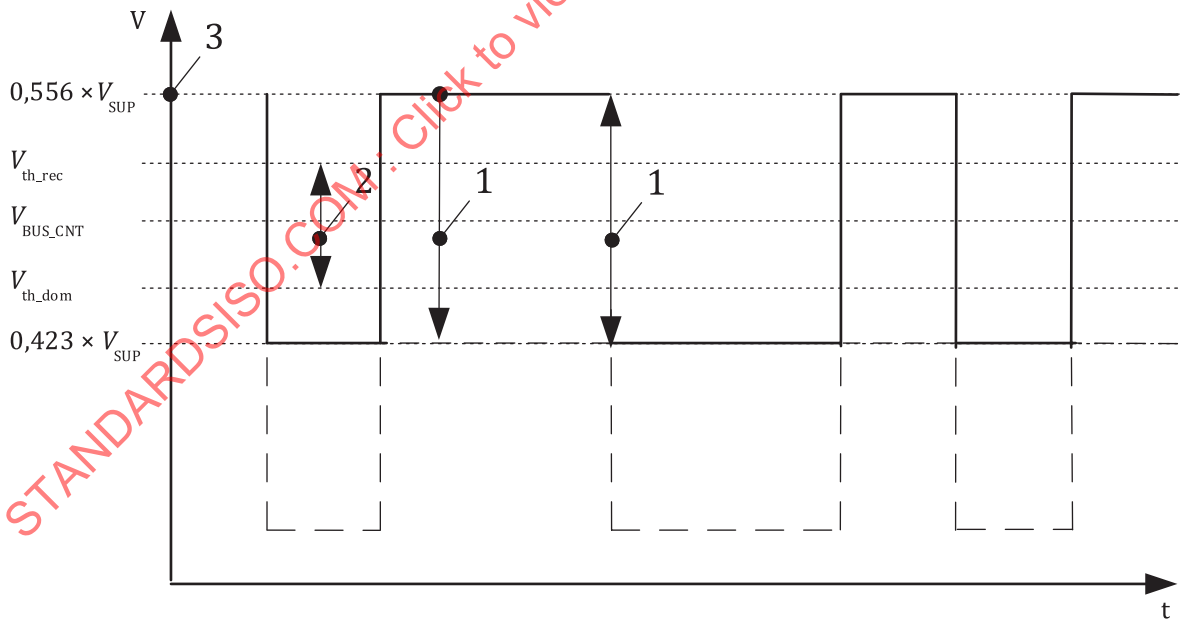


Key

1 V_{Dom_TS}
2 V_{HYS}
3 0,556 × V_{SUP} to 0,423 × V_{SUP} (signal voltage)
V voltage
t time

Figure 26 — Example of test (V_{Dom_TS} up) – Voltage threshold test 2

Figure 27 shows an example of test (V_{Rec_TS} down) – Voltage threshold test 2.



Key

1 V_{Dom_TS}
2 V_{HYS}
3 0,556 × V_{SUP} to 0,423 × V_{SUP} (signal voltage)
V voltage
t time

Figure 27 — Example of test (V_{Rec_TS} up) – Voltage threshold test 2

8.3.5 1.CTC_3.2 – Voltage threshold test 2

Table 66 specifies the CTC that verifies the 1.CTC_3.2 – Voltage threshold test 2.

Table 66 — 1.CTC_3.2 – Voltage threshold test 2

Item	Content
CTC # – Title	1.CTC_3.2 – Voltage threshold test 2
Purpose	This CTC verifies that the IUT operates the correct centre recessive threshold voltage.
Reference	ISO 20794-4:2020: — REQ 1.13 PHY – PMA electrical parameters V_{BUS_CNT}; — REQ 1.13 PHY – PMA electrical parameters V_{HYS}.
Prerequisite	The test system set-up shall be in accordance with Figure 25.
Set-up	— The IUT shall be configured as a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — V_{IUT} (V_{SUP} or V_{BAT}): see Table 67. — V_{Dom_TS}: see Table 67. — $V_{Rec\_TS}/V_{Pull\text{-}up}$: see Table 67. — R_{BUS}: see Table 67. — The LT shall set V_{Dom_TS} and V_{Rec_TS} according to Table 67 CTC_3.2-1.
Step	1. The TX_{PWM} data generator shall control the IUT to transmit and receive the PWM waveform. 2. The IUT shall vary the V_{Dom_TS} and the V_{Rec_TS} according to Table 67. 3. The measurement shall observe the PWM waveform and shall measure the voltage threshold, which does not set the transmission and reception cycle (V_{th_dom}, V_{th_rec}) and calculate the following parameter (see Figure 26 and Figure 27): — $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$; — $V_{HYS} = V_{th\_rec} - V_{th\_dom}$.
Iteration	Step 1 and step 2 shall be executed for each test case specified in Table 67.
Expected response	After step 1: The IUT shall transmit and receive the PWM waveform. During step 3: The measurement shall observe the PWM waveform and shall measure. The V_{BUS_CNT} shall be within [0,475 to 0,525] × V_{SUP}. The V_{HYS} shall be less than 0,133 × V_{SUP}.
Remark	---

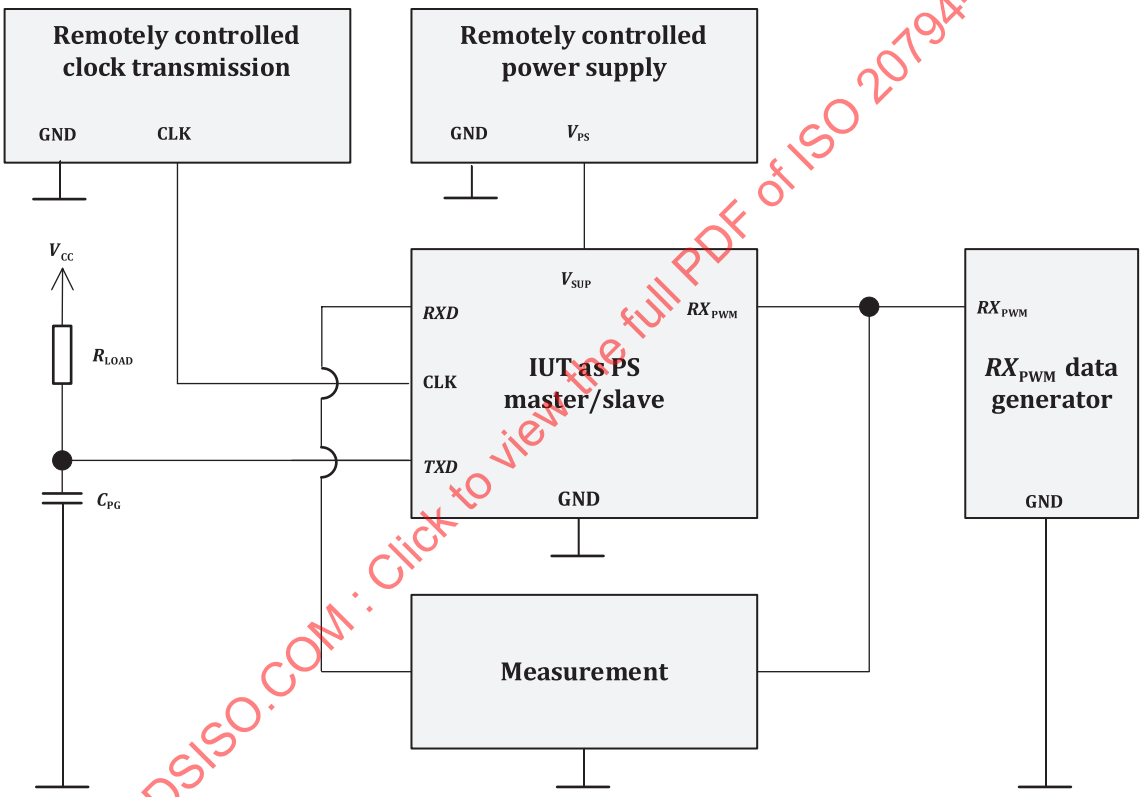
The V_{SUP} shall be calculated from the V_{BAT} by knowing the characteristic of the IUT.

Table 67 — TC – 1.CTC_3.2 – Voltage threshold voltage test 2

EPL-CT-TC	V_{IUT}	Amplitude	V_{Dom_TS}/V_{Rec_TS}	R_{BUS}	Test step
CTC_3.2-1	7 V	0,931 V	V_{Dom_TS} [2,961 V to 3,892 V] up	1 kΩ (±0,1 %)	The V_{Dom_TS}/V_{Rec} is varied by 0,02 V per step
			V_{Rec_TS} [3,892 V to 2,961 V] down		
CTC_3.2-2	13 V	1,729 V	V_{Dom_TS} [5,499 V to 7,228 V] up		
			V_{Rec_TS} [7,228 V to 5,499 V] down		
CTC_3.2-3	18 V	2,394 V	V_{Dom_TS} [7,614 V to 10,008 V] up		
			V_{Rec_TS} [10,008 V to 7,614 V] down		

8.3.6 1.CTC_3.3 – Duty cycle threshold test 1

This set-up of the test system is shown in Figure 28.



Components

C_{PG} capacitance

R_{LOAD} resistor of electric load

Figure 28 — Test system – Duty cycle threshold test set-up

Table 68 specifies the CTC that verifies the 1.CTC_3.3 – Duty cycle threshold test.

Table 68 — 1.CTC_3.3 – Duty cycle threshold test 1

Item	Content
CTC # – Title	1.CTC_3.3 – Duty cycle threshold test
Purpose	This CTC verifies that the decoding function complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 1.4 PHY – PS decoding function $t_{rx\_dif\_cont}$; — REQ 1.11 PHY – PS AC parameters $t_{rx\_0\_hi\_cont}$.
Prerequisite	The test system set-up shall be in accordance with Figure 28.
Set-up	— The IUT shall be configured as a master node (1.CTC_3.3-1 to 1.CTC_3.3-2) or a slave node (1.CTC_3.3-3 to 1.CTC_3.3-4). — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}]: 13 V. — *TXD*: — C_{PG} = 20 pF (±5 %); — R_{LOAD} = 2,4 kΩ (±5 %); — Pull-up resistor for open drain device only. — *Vcc*: The value depends on the tested device (5 V or 3,3 V).
Step	1. The RX_{PWM} data generator shall transmit the PWM waveform. The logical value 0 under the condition: $t_{rx\_0\_hi\_cont}$ = 1 µs and $t_{rx\_dif\_cont}$ = 2,5 µs.
Iteration	Step 1 shall be executed for each test case as specified in Table 69.
Expected response	After step 1: The IUT shall receive the PWM waveform.
Remark	---

The V_{SUP} shall be calculated from the V_{BAT} by knowing the characteristic of the IUT.

Table 69 — TC – 1.CTC_3.3 –Duty cycle threshold test 1

CTC-EPL-TC	$t_{rx\_0\_lo\_cont}$/$t_{rx\_0\_hi\_cont}$
1.CTC_3.3-1	$t_{rx\_0\_lo\_cont}$ = $t_{rx\_1\_lo\_cont}$ + 2,5 µs
1.CTC_3.3-2	$t_{rx\_0\_hi\_cont}$ = 1 µs
1.CTC_3.3-3	$t_{rx\_0\_lo\_cont}$ = $t_{rx\_1\_lo\_cont}$ + 2,5 µs
1.CTC_3.3-4	$t_{rx\_0\_hi\_cont}$ = 1µs

8.3.7 1.CTC_3.4 – Duty cycle threshold test 2

Table 70 specifies the CTC that verifies the 1.CTC_3.4 – Duty cycle threshold test 2.

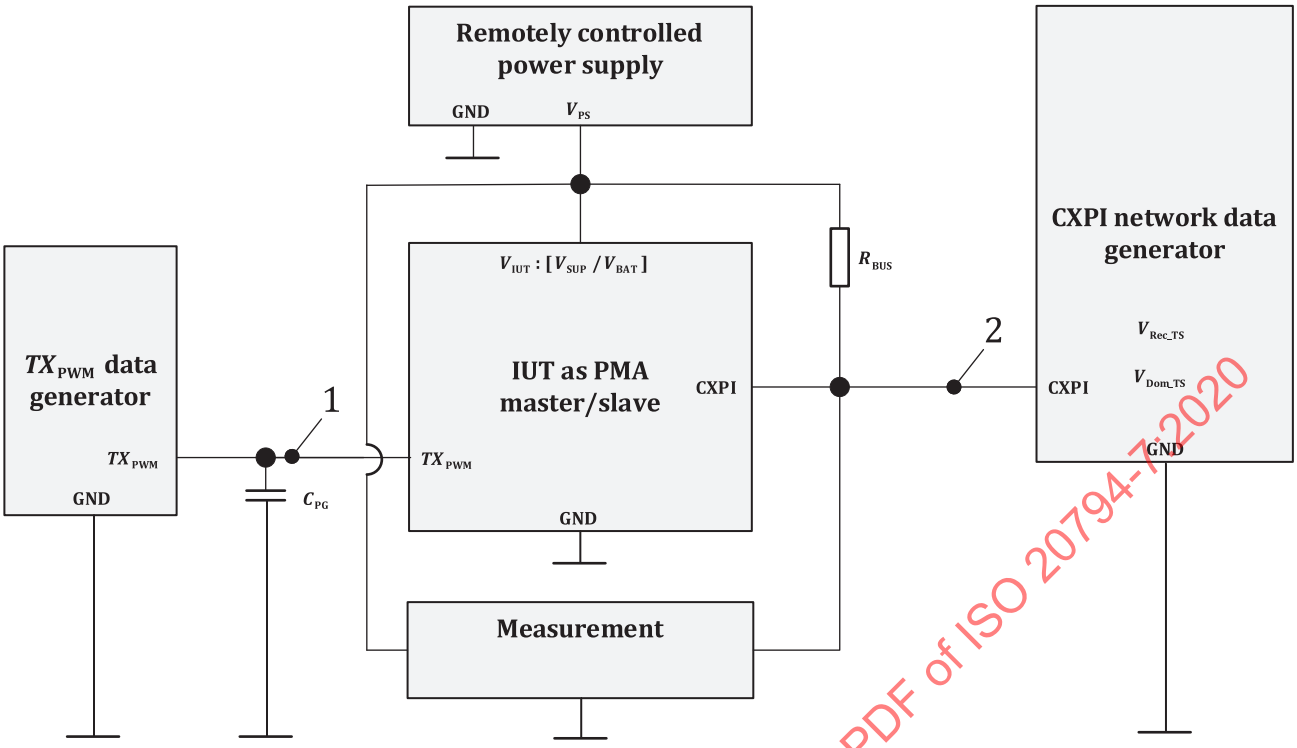
Table 70 — 1.CTC_3.4 – Duty cycle threshold test 2

Item	Content
CTC # – Title	1.CTC_3.4 – Duty cycle threshold test 2
Purpose	This CTC verifies that the decoding function complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 1.4 PHY – PS decoding function t_{sample_cont}.
Prerequisite	The test system set-up shall be in accordance with Figure 28.
Set-up	— The IUT shall be configured as a master node or a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}]: 13 V. — *TXD*: — C_{PG} = 20 pF (±5 %); — R_{LOAD} = 2,4 kΩ (±5 %); — Pull-up resistor for open drain device only. — *V*cc: The value shall depend on the tested device (5 V or 3,3 V).
Step	1. The RX_{PWM} data generator shall transmit the 10 bit of the logical value 1. 2. The RX_{PWM} data generator shall transmit the 1 bit of the logical value 1 waveform, which the LO width is 0,8 µs longer than step 1.
Iteration	Not applicable
Expected response	After step 1: The IUT shall receive the RX_{PWM} waveform as the logical value 1. After step 2: The IUT shall receive the RX_{PWM} waveform as the logical value 1.
Remark	---

8.4 CTP – Network state current characteristics

8.4.1 1.CTC_4.1 – Drive current test

The set-up for this test system is shown in Figure 29.



Key

1	TX_{PWM}
2	CXPI network
Components	
C_{PG}	capacitance
R_{BUS}	total CXPI network resistance

Figure 29 — Test system – Drive current test set-up

Table 71 specifies the CTC that verifies the 1.CTC_4.1 – Drive current test.

Table 71 — 1.CTC_4.1 – Drive current test

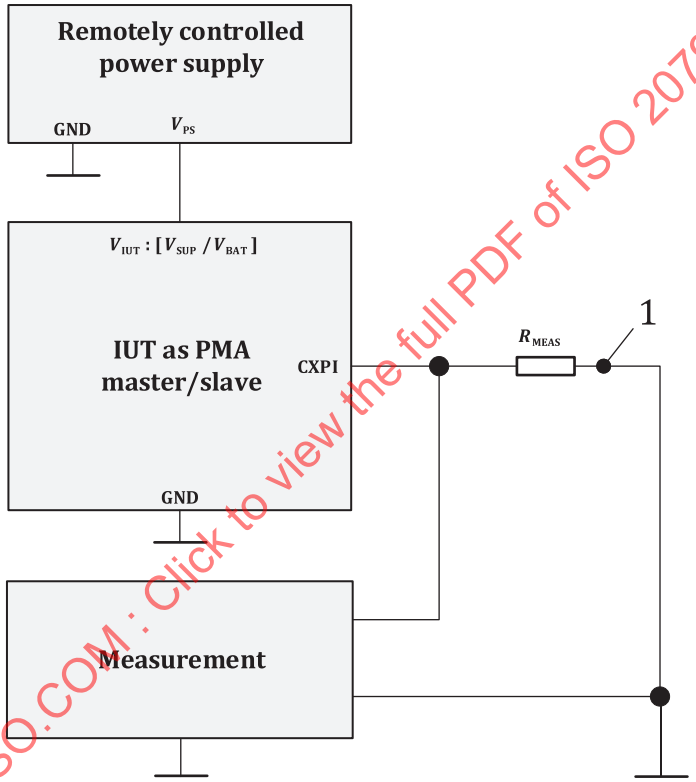
Item	Content
CTC # – Title	1.CTC_4.1 – Drive current test
Purpose	This CTC verifies that the drive capability of the IUT output.
Reference	ISO 20794-4:2020, REQ 1.13 PHY – PMA electrical parameters I_{BUS_LIM}.
Prerequisite	The test system set-up shall be in accordance with Figure 29.
Set-up	— The IUT shall be configured as a master node or a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}]: 18 V. — V_{Dom_TS}: 0 V. — V_{Rec_TS}: 18 V. — R_{BUS}: 440 Ω (±0,1 %). — TX_{PWM}: C_{PG} = 20 pF (±5 %).

Table 71 *(continued)*

Item	Content
Step	1. The TX_{PWM} data generator shall control the IUT to transmit and receive the PWM waveform.
Iteration	Not applicable
Expected response	After step 1: The measurement shall observe TH_{tx_dom} lower than 5,4 V as dominant level $TH_{tx\_dom} = 0{,}3 \times V_{IUT} = 5{,}4$ V.
Remark	---

8.4.2 1.CTC_4.2 – Input leakage test

The set-up for this test system is shown in Figure 30.



Key

1 CXPI network

Component

R_{MEAS} resistor for measurement

Figure 30 — Test system – Input leakage test set-up

Table 72 specifies the CTC that verifies the 1.CTC_4.2 – Input leakage test.

Table 72 — 1.CTC_4.2 – Input leakage test

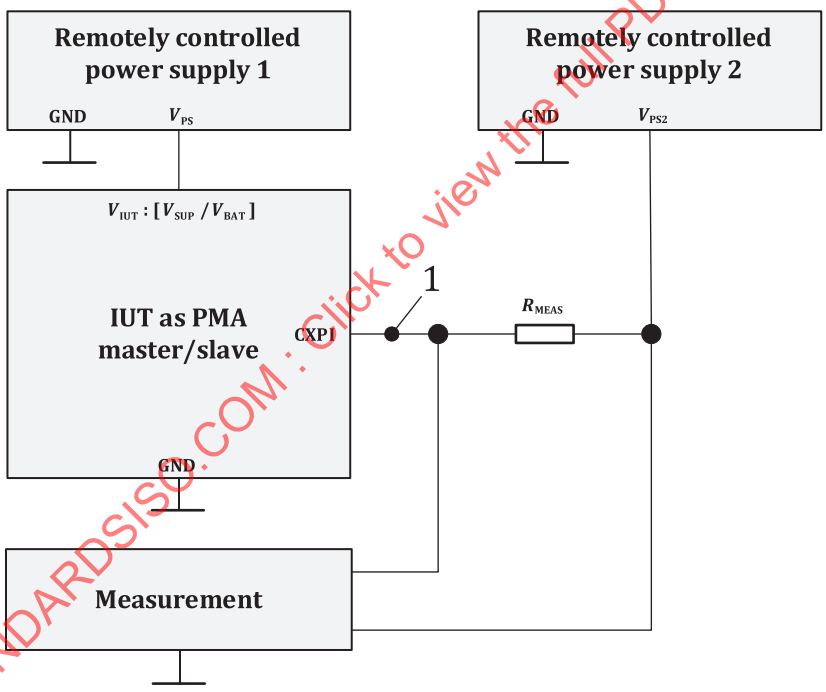
Item	Content
CTC # – Title	1.CTC_4.2 – Input leakage test
Purpose	This CTC verifies that the input leakage current $I_{BUS\_PAS\_dom}$ while the CXPI network is the dominant state complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 1.13 PHY –PMA electrical parameters $I_{BUS\_PAS\_dom}$.

Table 72 *(continued)*

Item	Content
Prerequisite	The test system set-up shall be in accordance with Figure 30.
Set-up	— The IUT shall be configured as a master node or a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}]: 12 V. — R_{MEAS}: 499 Ω (±0,1 %).
Step	1. The UT shall control the IUT to stop the transmission to the CXPI network.
Iteration	Not applicable
Expected response	After step 1: The measurement shall measure the maximum voltage drop value on the CXPI network which is higher than -500 mV.
Remark	---

8.4.3 1.CTC_4.3 – Reverse leakage current test

The set-up for this test system is shown in Figure 31.



Key

1	CXPI network
Component	
R_{MEAS}	resistor for measurement

Figure 31 — Test system – Reverse leakage current test set-up 1

Table 73 specifies the CTC that verifies the 1.CTC_4.3 – Reverse leakage current test.

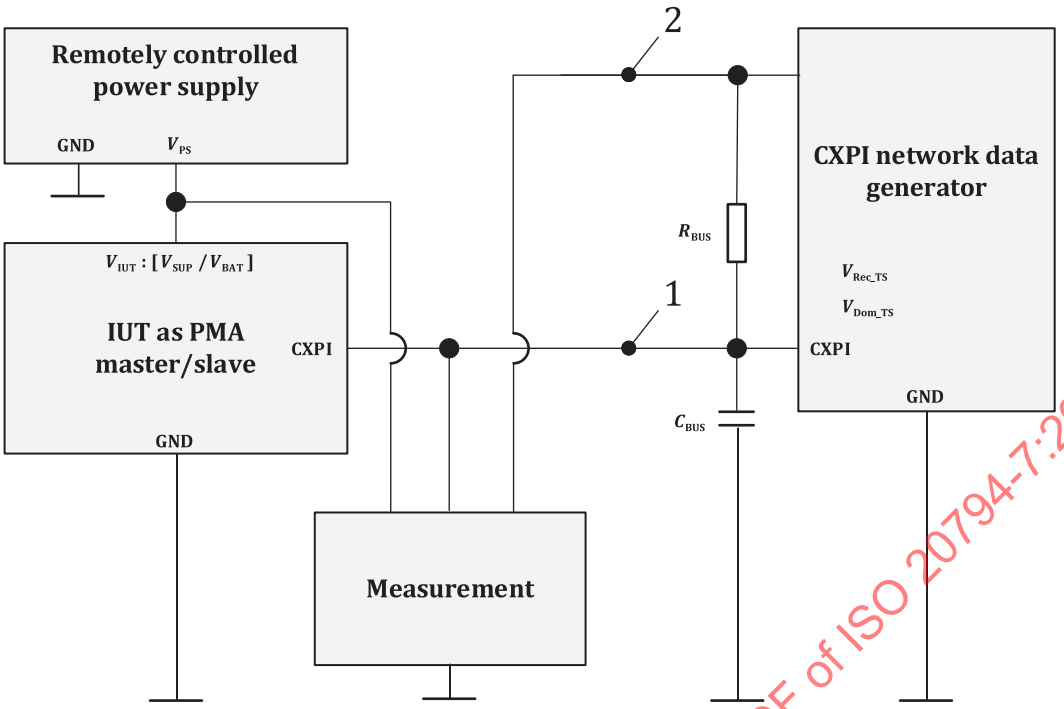
Table 73 — 1.CTC_4.3 – Reverse leakage current test

Item	Content
CTC # – Title	1.CTC_4.3 – Reverse leakage current test
Purpose	This CTC verifies that the reverse leakage current is limited to the maximum value of the $I_{BUS\_PAS\_rec}$ even if the V_{BUS} is higher than the IUT power voltage V_{IUT}.
Reference	ISO 20794-4:2020, REQ 1.13 PHY –PMA electrical parameters $I_{BUS\_PAS\_rec}$.
Prerequisite	The test system set-up shall be in accordance with Figure 31.
Set-up	— The IUT shall be configured as a master node or a slave node. — The bit rate shall be set to the default value (see 6.6.2). — V_{IUT}: [V_{SUP}/V_{BAT}]: 7,0 V/8,0 V. — R_{MEAS}: 1 000 Ω (±0,1 %). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to set a recessive level at the CXPI network terminal. 2. The remotely controlled power supply 2 shall increase or decrease V_{PS2} with a 2 V/s ramp in the range 8 V to 18 V.
Iteration	Not applicable
Expected response	After step 1: The measurement shall observe the maximum voltage drop value on the CXPI network which is less or equal than 20 mV.
Remark	---

8.5 CTP – Physical signal slope control

8.5.1 1.CTC_5.1 – Duty cycle measurement 1

The set-up for this test system is shown in Figure 32.



Key

1	CXPI network
2	$V_{\text{Pull-up}}$
Components	
C_{BUS}	total CXPI network capacitance
R_{BUS}	total CXPI network resistance

Figure 32 — Test system – Duty cycle measurement 1 test set-up

Table 74 specifies the CTC that verifies the 1.CTC_5.1 – Duty cycle measurement 1.

Table 74 — 1.CTC_5.1 – Duty cycle measurement 1

Item	Content
CTC # – Title	1.CTC_5.1 – Duty cycle measurement 1
Purpose	This CTC verifies that the duty cycle of the PWM waveform complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 1.5 PHY – PS clock generation; — REQ 1.14 PHY – PMA AC parameters $D_{\text{tx\_1\_lo\_dom}}$, $D_{\text{tx\_1\_lo\_rec}}$; — REQ 1.14 PHY – PMA AC parameters $D_{\text{tx\_0\_lo}}$; — REQ 1.15 PHY – PMA AC parameters – Param 32.
Prerequisite	The test system set-up shall be in accordance with Figure 32.

Table 74 *(continued)*

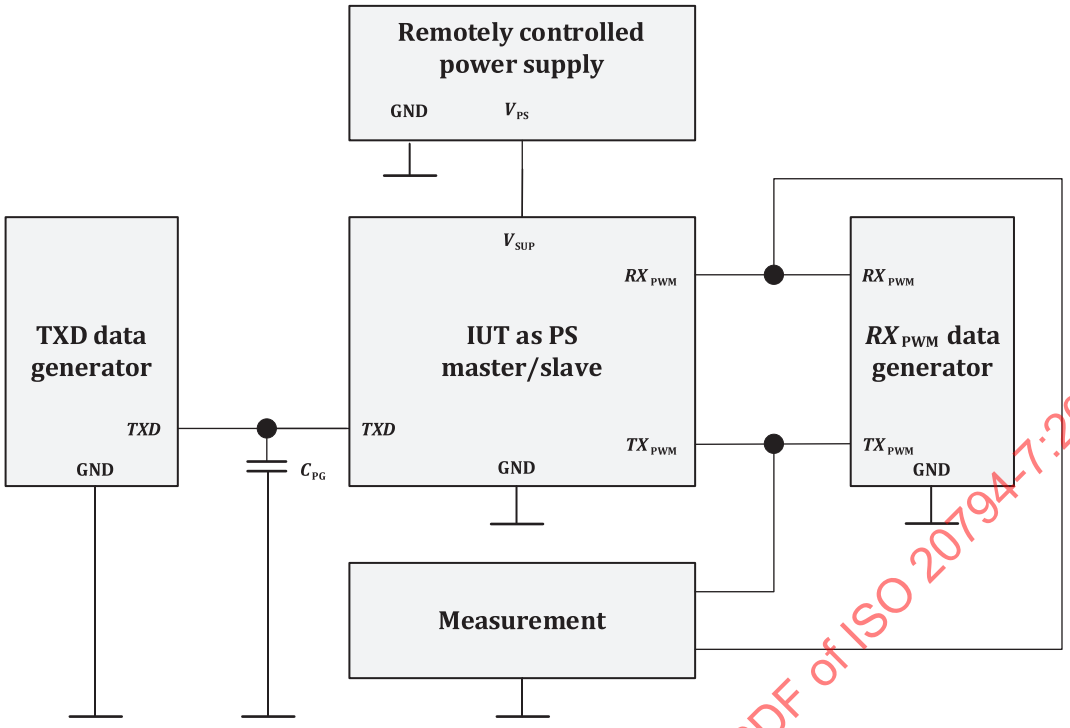
Item	Content
Set-up	— The IUT shall be configured as a master node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — CXPI network load: see Table 75. — V_{Dom_TS}: see Table 75. — $V_{Rec\_TS}/V_{Pull\text{-}up}$: see Table 75.
Step	1. The UT shall control the IUT to transmit a logical value 0 and 1 waveform.
Iteration	Step 1 shall be executed for each test case specified in Table 75.
Expected response	After step 1: The IUT shall transmit a logical value 0 and 1 waveform. The measurement shall observe and shall measure the waveform. The measured logical value 1 waveform shall be $D_{tx\_1\_lo\_dom} \geq 0{,}11$ and $D_{tx\_1\_lo\_rec} \leq 0{,}45$. The measured logical value 0 waveform shall be $D_{tx\_0\_lo} \geq D_{tx\_1\_lo} + 0{,}06$. The point of the waveform measurement shall be the start bit and the stop bit of the frame information field (L_FI) of the response.
Remark	---

Table 75 — TC – 1.CTC_5.1 – Duty cycle measurement 1

CTC-EPL-TC	V_{IUT}: [V_{SUP}/V_{BAT}]	$V_{Rec\_TS}/V_{Pull\text{-}up}$	CXPI network loads C_{BUS}/R_{BUS}
1.CTC_5.1-1	7,0 V/8,0 V	6,0 V	1 nF (±1 %)/1 kΩ (±0,1 %)
1.CTC_5.1-2	7,0 V/8,0 V	6,6 V	1 nF (±1 %)/1 kΩ (±0,1 %)
1.CTC_5.1-3	7,0 V/8,0 V	6,0 V	10 nF (±1 %)/500 Ω (±0,1 %)
1.CTC_5.1-4	7,0 V/8,0 V	6,6 V	10 nF (±1 %)/500 Ω (±0,1 %)
1.CTC_5.1-5	18 V/18,7 V	17,0 V	1 nF (±1 %)/1 kΩ (±0,1 %)
1.CTC_5.1-6	18 V/18,7 V	17,6 V	1 nF (±1 %)/1 kΩ (±0,1 %)
1.CTC_5.1-7	18 V/18,7 V	17,0 V	10 nF (±1 %)/500 Ω (±0,1 %)
1.CTC_5.1-8	18 V/18,7 V	17,6 V	10 nF (±1 %)/500 Ω (±0,1 %)

8.5.2 1.CTC_5.2 – Duty cycle measurement 2

The set-up for this test system is shown in Figure 33.



Component

C_{PG} capacitance

Figure 33 — Test system – Duty cycle measurement 2 test set-up

Table 76 specifies the CTC that verifies the 1.CTC_5.2 – Duty cycle measurement 2.

Table 76 — 1.CTC_5.2 – Duty cycle measurement 2

Item	Content
CTC # – Title	1.CTC_5.2 – Duty cycle measurement 2
Purpose	This CTC verifies that the PWM waveform of the TX_{PWM} complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 1.2 PHY – PS bit sample timing; — REQ 1.3 PHY – PS encoding function; — REQ 1.8 PHY – PS node clock synchronisation and bit synchronization.
Prerequisite	The test system set-up shall be in accordance with Figure 33.
Set-up	— The IUT shall be configured as a master node or a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — *TXD*: C_{PG} = 20 pF (±5 %).
Step	1. The *TXD* data generator shall control the IUT to transmit a logical value 0 and 1 waveform.
Iteration	Not applicable
Expected response	After step 1: The IUT shall transmit the logical value 0 and 1 waveform. The Measurement shall observe the waveform.
Remark	---

8.5.3 1.CTC_5.3 – Duty cycle measurement 3

Table 77 specifies the CTC that verifies the 1.CTC_5.3 – Duty cycle measurement 3.

Table 77 — 1.CTC_5.3 – Duty cycle measurement 3

Item	Content
CTC # – Title	1.CTC_5.3 – Duty cycle measurement 3
Purpose	This CTC verifies that the duty cycle of the PWM waveform complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 1.5 PHY – PS clock generation; — REQ 1.14 PHY – PMA AC parameters $D_{tx\_0\_lo}$; — REQ 1.15 PHY – PMA AC parameters – Param 32.
Prerequisite	The test system set-up shall be in accordance with Figure 32.
Set-up	— The IUT shall be configured as a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — CXPI network load: see Table 78. — V_{Dom_TS}: see Table 78. — $V_{Rec\_TS}/V_{Pull\text{-}up}$: see Table 78. — $t_{tx\_1\_lo\_dom\_TS} \approx t_{tx\_1\_lo\_rec\_TS}$: see Table 78.
Step	1. The CXPI network data generator shall transmit the clock in the logical 1 PWM waveform in various duty cycle [i.e. various Lo level width: $t_{tx\_1\_lo\_dom\_TS}$ ($\approx t_{tx\_1\_lo\_rec\_TS}$) shown in Table 78]. 2. The UT shall control the IUT to transmit the logical value 0.
Iteration	Step 1 shall be executed for each test case specified in Table 78.
Expected response	After step 1: The IUT shall transmit the logical value 0. The measurement shall observe and shall measure the waveform. The logical value 0 waveform shall be measured in the range of $D_{tx\_0\_lo} \geq D_{tx\_1\_lo} + 0{,}06$. The voltage level shall not exceed $0{,}3 \times V_{BUS}$ during the Lo width of a logical value 0 waveform. The point of the waveform measurement shall be the start bit and a stop bit of the frame information field (L_FI) of the response.
Remark	---

Table 78 — TC – 1.CTC_5.3 – Duty cycle measurement 3

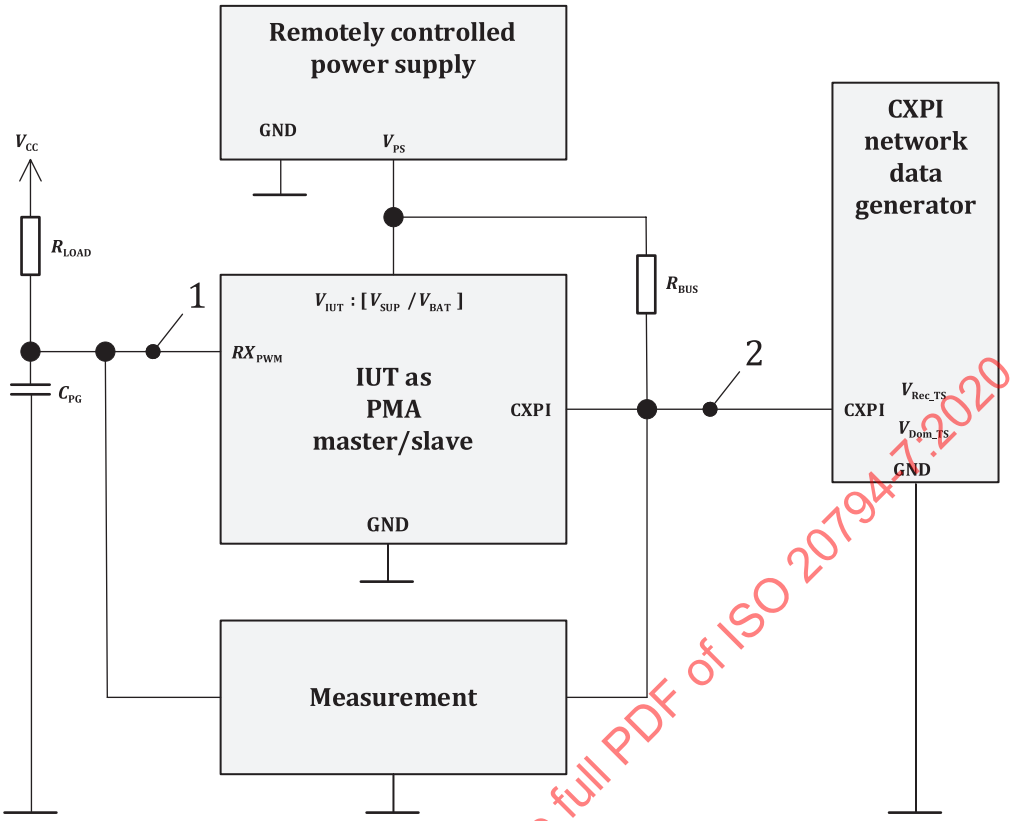
CTC-EPL-TC	V_{IUT}: [V_{SUP}/V_{BAT}]	V_{Rec_TS}/ $V_{Pull\text{-}up}$	CXPI network loads C_{BUS}/R_{BUS}	Duty cycle $t_{tx\_1\_lo\_dom\_TS}$ $t_{tx\_1\_lo\_rec\_TS}$
1.CTC_5.3-1	7,0 V/8,0 V	6,0 V	1 nF (±1 %)/1 kΩ (±0,1 %)	$t_{tx\_1\_lo\_dom\_TS} = 0{,}11\ t_{bit}$
1.CTC_5.3-2	7,0 V/8,0 V	6,6 V	1 nF (±1 %)/1 kΩ (±0,1 %)	
1.CTC_5.3-3[a]	7,0 V/8,0 V	6,0 V	10 nF (±1 %)/500 Ω (±0,1 %)	
1.CTC_5.3-4[a]	7,0 V/8,0 V	6,6 V	10 nF (±1 %)/500 Ω (±0,1 %)	
1.CTC_5.3-5	18 V/18,7 V	17,0 V	1 nF (±1 %)/1 kΩ (±0,1 %)	
1.CTC_5.3-6	18 V/18,7 V	17,6 V	1 nF (±1 %)/1 kΩ (±0,1 %)	
1.CTC_5.3-7[a]	18 V/18,7 V	17,0 V	10 nF (±1 %)/500 Ω (±0,1 %)	
1.CTC_5.3-8[a]	18 V/18,7 V	17,6 V	10 nF (±1 %)/500 Ω (±0,1 %)	
1.CTC_5.3-9	7,0 V/8,0 V	6,0 V	1 nF (±1 %)/1 kΩ (±0,1 %)	$t_{tx\_1\_lo\_rec\_TS} = 0{,}39\ t_{bit} + 0{,}6\ \tau$
1.CTC_5.3-10	7,0 V/8,0 V	6,6 V	1 nF (±1 %)/1 kΩ (±0,1 %)	
1.CTC_5.3-11	7,0 V/8,0 V	6,0 V	10 nF (±1 %)/500 Ω (±0,1 %)	
1.CTC_5.3-12	7,0 V/8,0 V	6,6 V	10 nF (±1 %)/500 Ω (±0,1 %)	
1.CTC_5.3-13	18 V/18,7 V	17,0 V	1 nF (±1 %)/1 kΩ (±0,1 %)	
1.CTC_5.3-14	18 V/18,7 V	17,6 V	1 nF (±1 %)/1 kΩ (±0,1 %)	
1.CTC_5.3-15	18 V/18,7 V	17,0 V	10 nF (±1 %)/500 Ω (±0,1 %)	
1.CTC_5.3-16	18 V/18,7 V	17,6 V	10 nF (±1 %)/500 Ω (±0,1 %)	

[a] If 1.CTC_5.3-11, 1.CTC_5.3-12, 1.CTC_5.3-15 and 1.CTC_5.3-16 pass, this test case is optional.

8.5.4 1.CTC_5.4 – Propagation delay of the receiver test

This test is applicable only to the IUT which has the RX_{PWM} terminal.

This set-up of the test system is shown in Figure 34.



Key

1	RX_{PWM}
2	CXPI network
Components	
C_{PG}	capacitance
R_{LOAD}	resistor of electric load
R_{BUS}	total CXPI network resistance

Figure 34 — Test system – Propagation delay of the receiver test set-up

Table 79 specifies the CTC that verifies the 1.CTC_5.4 – Propagation delay of the receiver test.

Table 79 — 1.CTC_5.4 – Propagation delay of the receiver test

Item	Content
CTC # – Title	1.CTC_5.4 – Propagation delay of the receiver test
Purpose	This CTC verifies that the propagation delay of the receiving node of the IUT complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 1.14 PHY – PMA AC parameters $t_{rx\_pwm\_pd}$; — REQ 1.14 PHY – PMA AC parameters $t_{rx\_pwm\_pd\_sym}$.
Prerequisite	The test system set-up shall be in accordance with Figure 34.

Table 79 *(continued)*

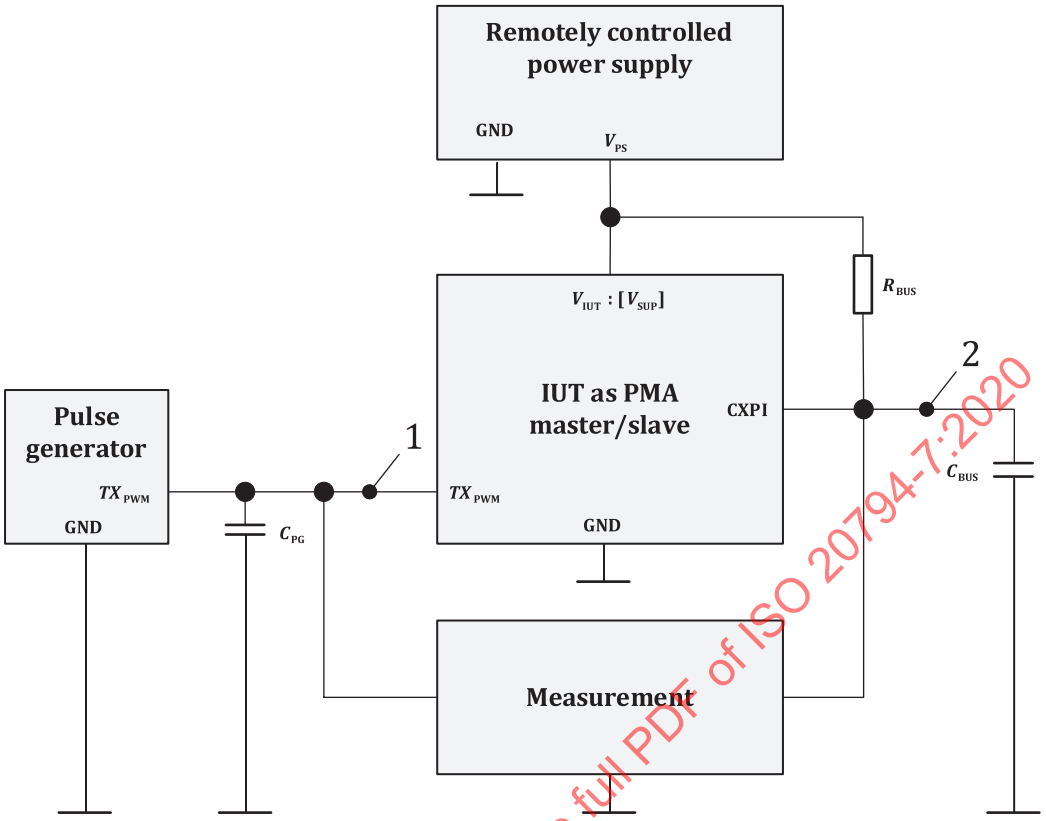
Item	Content
Set-up	— The IUT shall be configured as a master node (1.CTC_5.4-1 to 1.CTC_5.4-3) or a slave node (1.CTC_5.4-1 to 1.CTC_5.4-3). — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — V_{IUT}: [V_{SUP}]: see Table 80. — *RX*: — C_{PG} = 20 pF (±5 %); — R_{LOAD} = 2,4 kΩ (±5 %); — Pull-up resistor for open drain device only. — *Vcc*: value depends on the tested device (5 V or 3,3 V). — R_{BUS}: 1kΩ (±0,1 %).
Step	1. The CXPI network data generator shall be driven with a 50 % duty cycle square wave at 10 kHz.
Iteration	Step 1 shall be executed for each test case specified in Table 80.
Expected response	After step 2: The measurement shall observe the RX_{PWM} and shall measure the RX_{PWM} waveform. The IUT shall be a master node. Measured time $t_{rx\_pwm\_pd}$ shall be less than 2,1 µs. The IUT shall be a slave node. Measured time $t_{rx\_pwm\_pd\_sym}$ shall be within ±2 µs.
Remark	---

Table 80 — TC – 1.CTC_5.4 – Propagation delay of the receiver test

CTC-EPL-TC	V_{IUT}: [V_{SUP}]
1.CTC_5.4-1	7 V
1.CTC_5.4-2	13 V
1.CTC_5.4-3	18 V

8.5.5 1.CTC_5.5 – Propagation delay of the transmitter test

This test is applicable only to the IUT, which has a TX terminal. This set-up of the test system is shown in Figure 35.



Key

1	TX_{PWM}
2	CXPI network
Components	
C_{PG}	capacitance
R_{BUS}	total CXPI network resistance

Figure 35 — Test system – Propagation delay of the transmitter test set-up

Table 81 specifies the CTC that verifies the 1.CTC_5.5 – Propagation delay of the transmitter test.

Table 81 — 1.CTC_5.5 – Propagation delay of the transmitter test

Item	Content
CTC # – Title	1.CTC_5.5 – Propagation delay of the transmitter test
Purpose	This CTC verifies that the propagation delay of the transmitter of the IUT complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 1.14 PHY – PMA AC parameters $t_{tx\_pwm\_pdf}$; — REQ 1.14 PHY – PMA AC parameters $t_{tx\_pwm\_pdr}$; — REQ 1.14 PHY – PMA AC parameters $t_{tx\_pwm\_pdf\_clk}$.
Prerequisite	The test system set-up shall be in accordance with Figure 35.

Table 81 *(continued)*

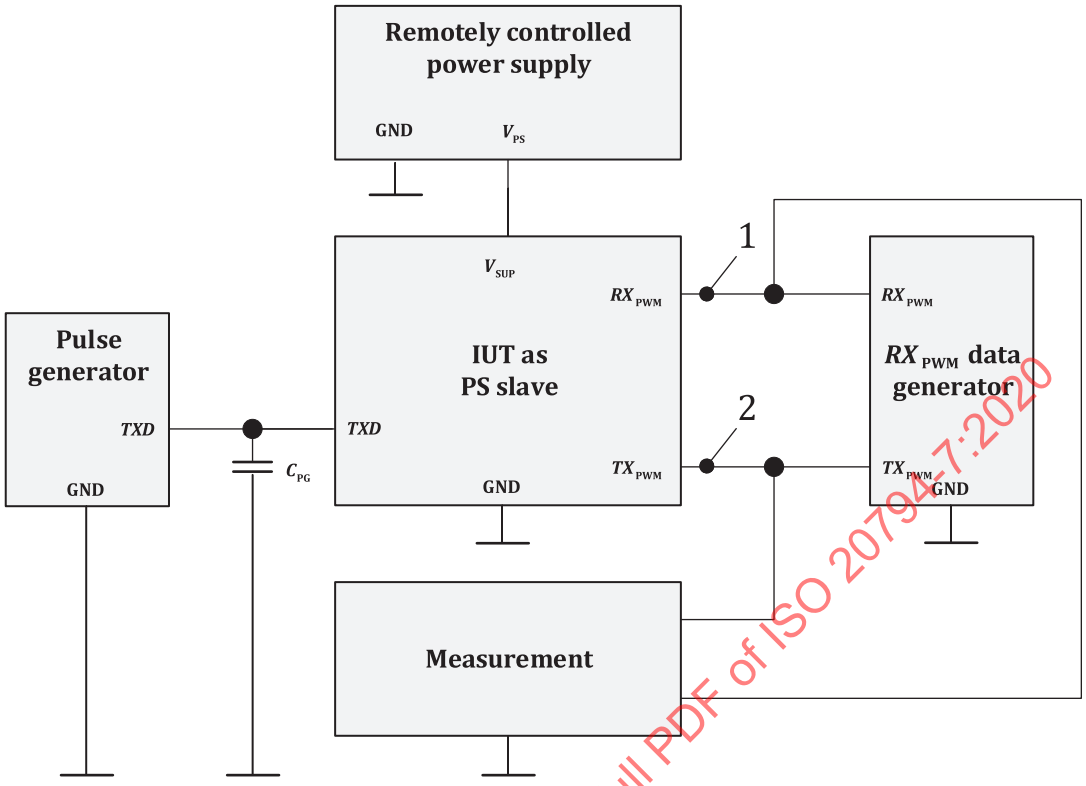
Item	Content
Set-up	— The IUT shall be configured as a master node (1.CTC_5.5-1 to 1.CTC_5.5-6) or a slave node (1.CTC_5.5-1 to 1.CTC_5.5-6). — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — V_{IUT}: [V_{SUP}]: see Table 82. — *TX*: C_{PG} = 20 pF (±5 %).
Step	1. The pulse generator shall be driven with a 50 % duty cycle square wave at 10 kHz.
Iteration	Step 1 shall be executed for each test case specified in Table 82.
Expected response	After step 1: The measurement shall observe and shall measure the PWM waveform. IUT shall be in the master node or the slave node. Measured time $t_{tx\_pwm\_pdf}$ shall be less than 2,9 µs. IUT shall be in the slave node. Measured time $t_{tx\_pwm\_pdr}$ shall be less than 16,9 µs. IUT shall be in the master node. Measured time $t_{tx\_pwm\_pdf\_clk}$ shall be less than 16,9 µs.
Remark	---

Table 82 — TC – 1.CTC_5.5 – Propagation delay of the transmitter test

CTC-EPL-TC	V_{IUT}: [V_{SUP}]	CXPI network loads C_{BUS}/R_{BUS}
1.CTC_5.5-1	7,0 V	1 nF (±1 %)/1 kΩ (±0,1 %)
1.CTC_5.5-2	7,0 V	10 nF (±1 %)/500 Ω (±0,1 %)
1.CTC_5.5-3	13 V	1 nF (±1 %)/1 kΩ (±0,1 %)
1.CTC_5.5-4	13 V	10 nF (±1 %)/500 Ω (±0,1 %)
1.CTC_5.5-5	18 V	1 nF (±1 %)/1 kΩ (±0,1 %)
1.CTC_5.5-6	18 V	10 nF (±1 %)/500 Ω (±0,1 %)

8.5.6 1.CTC_5.6 – Propagation delay of the transmitter test 2

This set-up of the test system is shown in Figure 36.



Key

1	RX_{PWM}
2	TX_{PWM}
Component	
C_{PG}	capacitance

Figure 36 — Test system - Propagation delay of the transmitter test 2 set-up

Table 83 specifies the CTC that verifies the 1.CTC_5.6 – Propagation delay of the transmitter test 2.

Table 83 — 1.CTC_5.6 – Propagation delay of the transmitter test 2

Item	Content
CTC # – Title	1.CTC_5.6 – Propagation delay of the transmitter test 2
Purpose	This CTC verifies that the propagation delay of the transmitter of the IUT complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 1.11 PHY – PS AC parameters $T_{tx\_0\_pd\_cont}$.
Prerequisite	The test system set-up shall be in accordance with Figure 36.
Set-up	— The IUT shall be configured as a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — V_{IUT}: [V_{SUP}]: 13 V. — *TXD*: C_{PG} = 20 pF (±5 %).
Step	1. The RX_{PWM} data generator shall start transmitting the clock as a waveform. 2. The pulse generator shall be driven with a 50 % duty cycle square wave at 10 kHz.

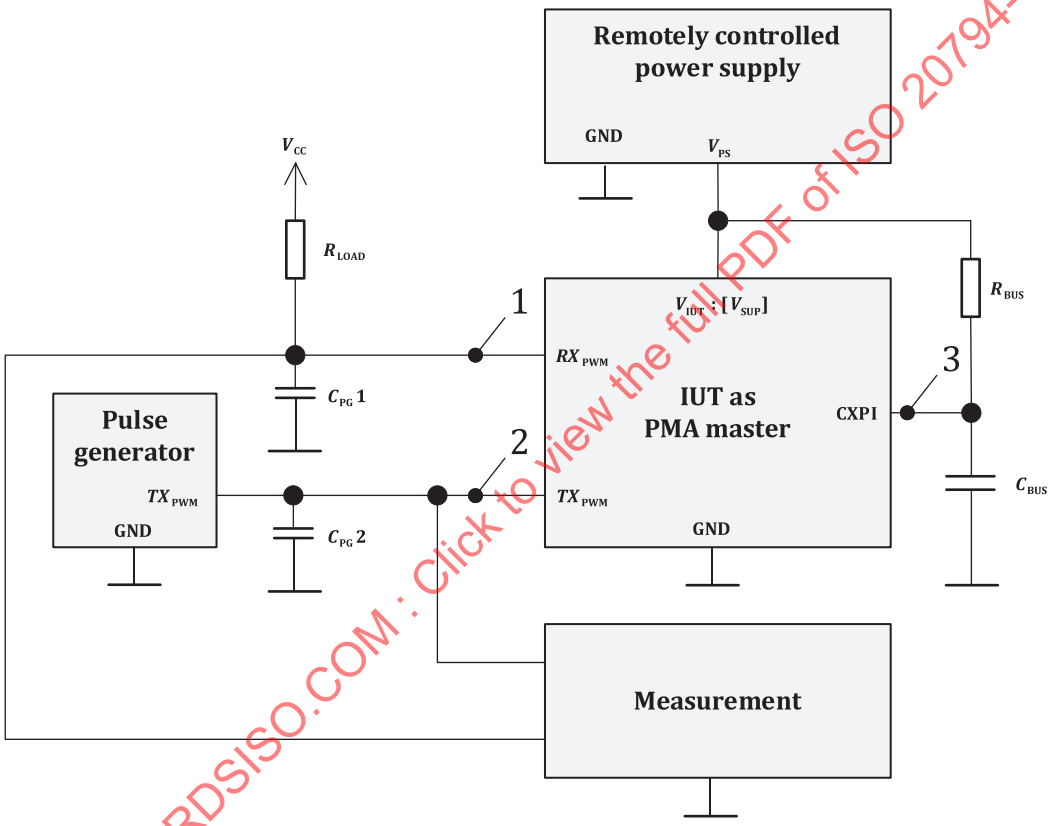
Table 83 *(continued)*

Item	Content	
Expected response	After step 2:	The IUT shall transmit the TX_{PWM} waveform. The measurement shall observe and shall measure the PWM waveform at the time from a falling edge of the RX_{PWM} to a falling edge of the TX_{PWM}, and the measured time $t_{tx\_pwm\_pdr}$ shall be less than 0,5 µs.
Remark	---	

8.5.7 1.CTC_5.7 – Loop back time test

This test is applicable only to IUT which has the RX_{PWM} terminal and the TX_{PWM} terminal.

This set-up of the test system is shown in Figure 37.



Key

1	RX_{PWM}
2	TX_{PWM}
3	CXPI network
Components	
C_{PG1}	capacitance
C_{PG2}	capacitance
R_{LOAD}	resistor of electric load
C_{BUS}	total CXPI network capacitance
R_{BUS}	total CXPI network resistance

Figure 37 — Test system – Loop back time test set-up

Table 84 specifies the CTC that verifies the 1.CTC_5.7 – Loop back time test.

Table 84 — 1.CTC_5.7 – Loop back time test

Item	Content
CTC # – Title	1.CTC_5.7 – Loop back time test
Purpose	This CTC verifies that the loop back of the transmitter of the IUT complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 1.14 PHY – PMA AC parameters $t_{loop\_pwm\_pd}$.
Prerequisite	The test system set-up shall be in accordance with Figure 37.
Set-up	— The IUT shall be configured as a master node (1.CTC_5.7-1 to 1.CTC_5.7-3). — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — V_{IUT}: [V_{SUP}]: see Table 85. — *RX*: — $C_{PG}1$ = 20 pF (±5 %); — R_{LOAD} = 2,4 kΩ (±5 %); — Pull-up resistor for open drain device only. — *TX*: $C_{PG}2$ = 20 pF (±5 %). — *Vcc*: The value depends on the tested device (5 V or 3,3 V).
Step	1. The pulse generator shall be driven with a 50 % duty cycle square wave at 10 kHz.
Iteration	Step 1 shall be executed for each test case specified in Table 85.
Expected response	After step 1: The measurement shall observe and shall measure the TX_{PWM} and the RX_{PWM} waveform and measure the time t_{loop_pwm}, whether it is less than 19,0 µs.
Remark	---

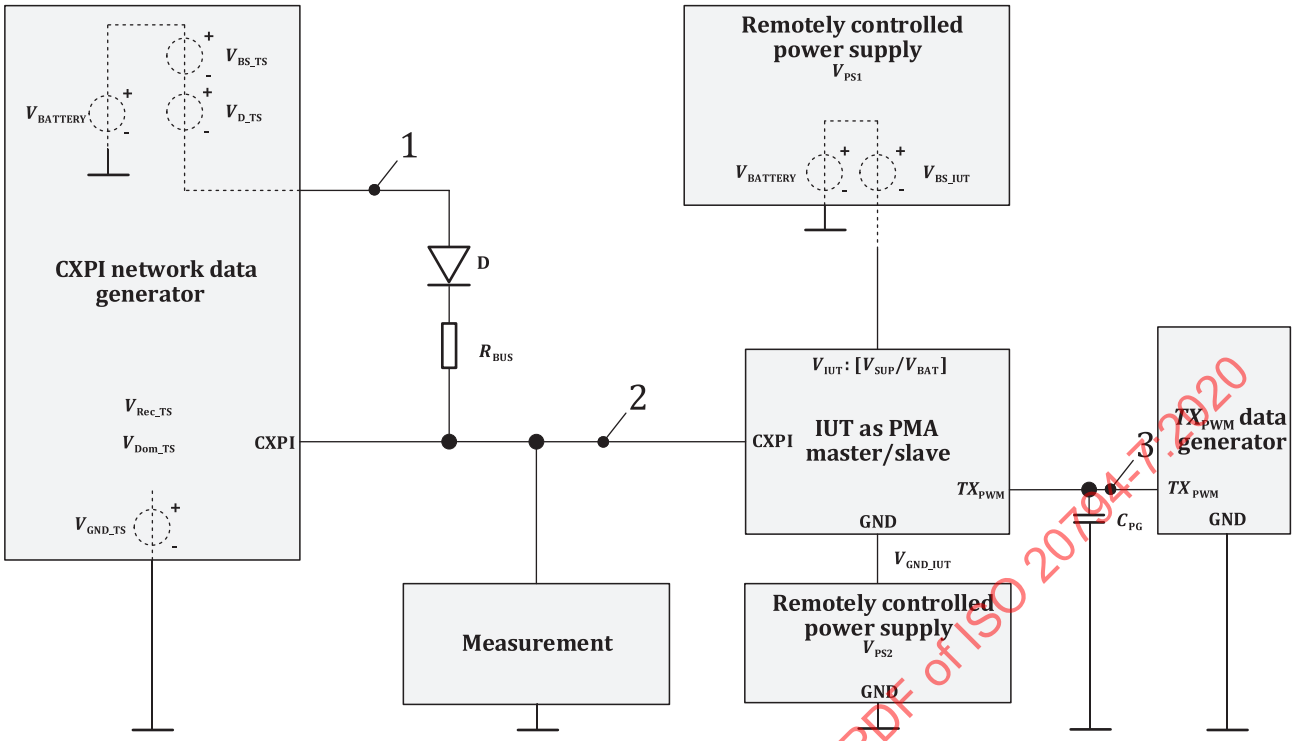
Table 85 — TC – 1.CTC_5.7 – Loop back time test

CTC-EPL-TC	V_{IUT}: [V_{SUP}]	CXPI network loads C_{BUS}/R_{BUS}
1.CTC_5.7-1	7,0 V	1 nF (±1 %)/1 kΩ (±0,1 %)
1.CTC_5.7-2	7,0 V	10 nF (±1 %)/500 Ω (±0,1 %)
1.CTC_5.7-3	13 V	1 nF (±1 %)/1 kΩ (±0,1 %)

8.6 CTP – GND/V_{BAT} shift test

8.6.1 GND/V_{BAT} shift test set-up

This CTC verifies the robustness in case of V_{BAT} and GND shift. Figure 38 shows the test system – GND/V_{BAT} shift test set-up.



Key

1	$V_{\text{Pull-up}}$
2	CXPI network
3	TX_{PWM}
Components	
D	Diode (1N4148)
C_{PG}	capacitance
R_{BUS}	total CXPI network resistance

Figure 38 — Test system – GND/V_{BAT} shift test set-up

8.6.2 1.CTC_6.1 – GND shift test

Table 86 specifies the CTC that verifies the 1.CTC_6.1 – GND shift test.

Table 86 — 1.CTC_6.1 – GND shift test

Item	Content
CTC # – Title	1.CTC_6.1 – GND shift test
Purpose	This CTC verifies that the robustness in case of the GND shift complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 1.13 PHY – PMA electrical parameters $V_{\text{Shift\_GND}}$; — REQ 1.13 PHY – PMA electrical parameters $V_{\text{Shift\_Difference}}$.
Prerequisite	The test system set-up shall be in accordance with Figure 38.

Table 86 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a master node or a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — $V_{BATTERY:}$ 8,96 V. — $V_{BS\_TS:}$ 0,1 × 8 V. — $V_{D\_TS:}$ 1 V. — $V_{GND\_TS:}$ 0,02 × $V_{BATTERY.}$ — $V_{Rec\_TS}/V_{Pull\text{-}up}$: 0,7 × ($V_{BATTERY}$ - V_{BS_TS} - V_{D_TS} - V_{GND_TS}). — V_{Dom_TS}: 0,3 × ($V_{BATTERY}$ - V_{BS_TS} - V_{D_TS} - V_{GND_TS}). — V_{BS_IUT}: 0 V. — V_{IUT}: $V_{BATTERY}$ - V_{BS_IUT} - $V_{GND\_IUT.}$ — V_{GND_IUT}: 0,08 × 8 V. — R_{BUS}: see Table 87. — TX_{PWM}: C_{PG} = 20 pF (±5 %).
Step	1. The IUT shall set the R_{BUS} for each type according to Table 87. 2. The UT shall control the IUT to transmit and receive the PWM waveform.
Iteration	Not applicable
Expected response	After step 2: The IUT shall transmit and receive the PWM waveform.
Remark	---

Table 87 — TC – 1.CTC_6.1 – GND shift test

CTC-EPL-TC	IUT type	R_{BUS}
1.CTC_6.1-1	Master node	30 kΩ (±0,1 %)
	Slave node	1 kΩ (±0,1 %)

8.6.3 1.CTC_6.2 – V_{BAT} shift test

Table 88 specifies the CTC that verifies the 1.CTC_6.2 – V_{BAT} shift test.

Table 88 — 1.CTC_6.2 – V_{BAT} shift test

Item	Content
CTC # – Title	1.CTC_6.2 – V_{BAT} shift test
Purpose	This CTC verifies that the robustness in case of V_{BAT} shift complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 1.13 PHY – PMA electrical parameters V_{Shift_BAT}; — REQ 1.13 PHY – PMA electrical parameters $V_{Shift\_Difference}$.
Prerequisite	The test system set-up shall be in accordance with Figure 38.

Table 88 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a master node or a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — $V_{BATTERY:}$ 8,96 V. — $V_{BS\_TS:}$ 0,02 × 8 V. — $V_{D\_TS:}$ 0,4 V. — $V_{GND\_TS:}$ 0,1 × 8 V. — $V_{Rec\_TS}/V_{Pull\text{-}up:}$ 0,7 × ($V_{BATTERY}$ - V_{BS_TS} - V_{D_TS} - V_{GND_TS}). — $V_{Dom\_TS:}$ 0,3 × ($V_{BATTERY}$ - V_{BS_TS} - V_{D_TS} - V_{GND_TS}). — $V_{BS\_IUT:}$ 0,08 × 8 V. — $V_{IUT:}$ $V_{BATTERY}$ - V_{BS_IUT} - V_{GND_IUT}. — $V_{GND\_IUT:}$ 0 V. — R_{BUS}: see Table 89. — TX_{PWM}: C_{PG} = 20 pF (±5 %).
Step	1. The IUT shall set the R_{BUS} for each type according to Table 89. 2. The UT shall control the IUT to transmit and receive the PWM waveform.
Iteration	Not applicable
Expected response	After step 2: The IUT shall transmit and receive the PWM waveform.
Remark	---

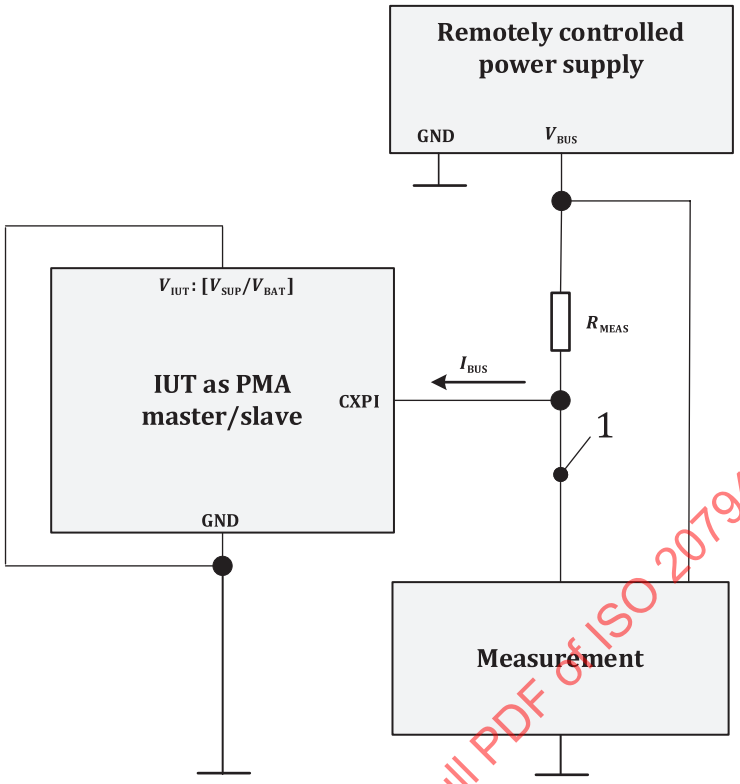
Table 89 — TC – 1.CTC_6.2 – V_{BAT} shift test

CTC-EPL-TC	IUT type	R_{BUS}
1.CTC_6.2-1	Master node	30 kΩ (±0,1 %)
	Slave node	1 kΩ (±0,1 %)

8.7 CTP – Loss of power supply

8.7.1 Loss of battery and Loss of GND test set-up

The set-up for this test system is shown in Figure 39.



Key

1	CXPI network
Component	
R_{MEAS}	resistor for measurement

Figure 39 — Test system – Loss of battery test (V_{BAT}) test set-up

8.7.2 1.CTC_7.1 – Loss of battery test (V_{BAT})

Table 90 specifies the CTC that verifies the 1.CTC_7.1 – Loss of battery test (V_{BAT}).

Table 90 — 1.CTC_7.1 – Loss of battery test (V_{BAT})

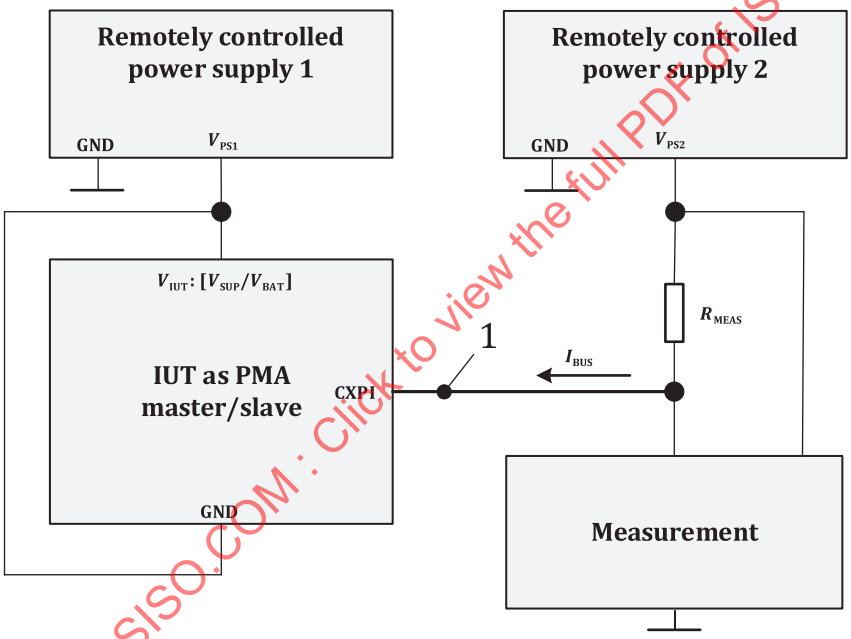
Item	Content
CTC # – Title	1.CTC_7.1 – Loss of battery test (V_{BAT})
Purpose	This CTC verifies that the behaviour of the IUT when it loses the battery voltage complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 1.13 PHY – PMA electrical parameters $I_{BUS\_NO\_BAT}$.
Prerequisite	The test system set-up shall be in accordance with Figure 39.
Set-up	— The IUT shall be configured as a master node or a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to L_PwrMng1 (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}] = GND. — Failure: Loss of Battery (V_{BAT}). — V_{BUS}: 0 < V_{BUS} < 18 V. — $R_{MEAS:}$ 10 kΩ (±0,1 %).

Table 90 *(continued)*

Item	Content
Step	1. The IUT shall disconnect the power supply from the V_{IUT} terminal of the IUT. 2. The remotely controlled power supply shall increase or decrease V_{BUS} with a 2 V/s ramp in the range 0 V to 18 V. 3. The IUT shall connect the power supply from the V_{IUT} terminal of the IUT.
Iteration	Not applicable
Expected response	After step 2: The measurement shall observe and measures the I_{BUS}. I_{BUS} shall be less than 100 µA (i.e. voltage drop less than 1 V). After Step 3 The IUT shall restart.
Remark	---

8.7.3 1.CTC_7.2 – Loss of GND test

The set-up for this test system is shown in Figure 40.



Key

1	CXPI network
Component	
R_{MEAS}	resistor for measurement

Figure 40 — Test system – Loss of GND test set-up

Table 91 specifies the CTC that verifies the 1.CTC_7.2 – Loss of *GND* test.

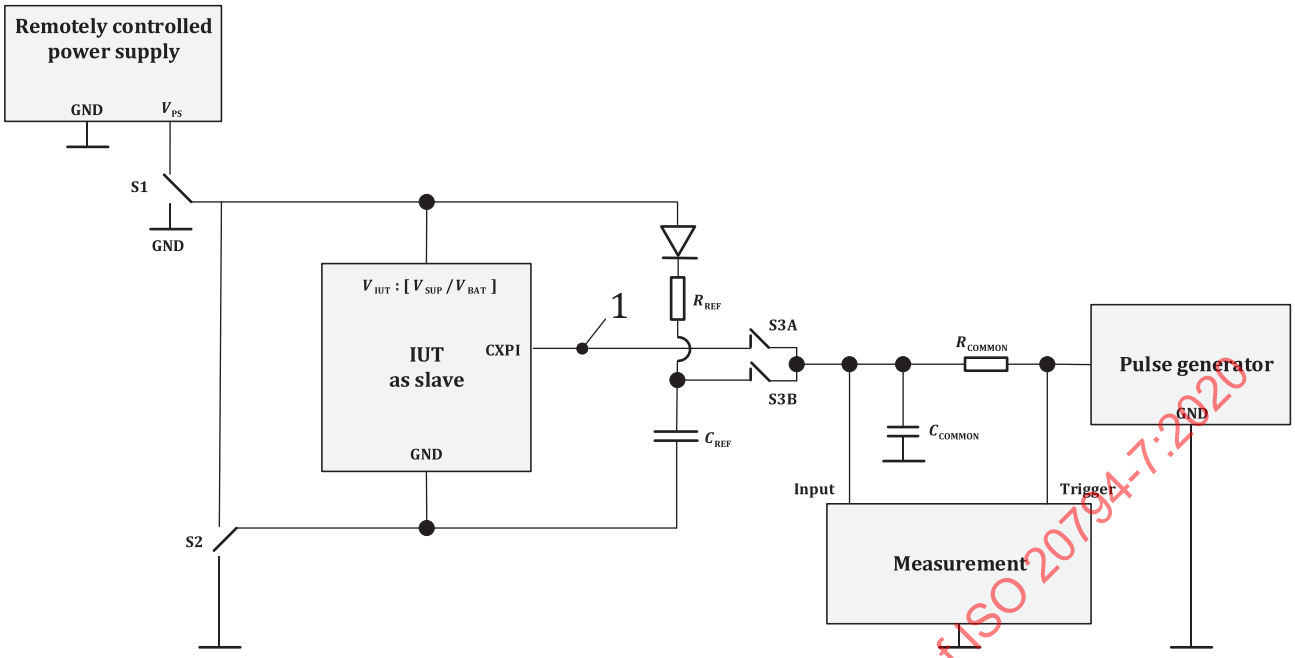
Table 91 — 1.CTC_7.2 – Loss of GND test

Item	Content
CTC # – Title	1.CTC_7.2 – Loss of *GND* test
Purpose	This CTC verifies that the behaviour of the IUT when it loses the GND complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 1.13 PHY – PMA electrical parameters $I_{BUS\_NO\_GND}$.
Prerequisite	The test system set-up shall be in accordance with Figure 40.
Set-up	— The IUT shall be configured as a master node or a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to L_PwrMng1 (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}]: V_{IUT} = V_{PS1} = 12 V. — GND = V_{IUT}: GND of the IUT shorts out to V_{IUT}. — Failure: loss of GND. — R_{MEAS}: 1 kΩ (±0,1 %).
Step	1. The IUT shall disconnect the GND. 2. The remotely controlled power supply shall increase or decrease V_{PS2} with a 2 V/s ramp in the range 0 V to 18 V. 3. The IUT shall connect the GND to the IUT.
Iteration	Not applicable
Expected response	After step 2: The measurement shall observe and measure the I_{BUS}. I_{BUS} shall be in the range of ±1 mA (i.e. R_{MEAS} (≦1 kΩ) is voltage drop less than 1 V). After step 3: The IUT shall restart.
Remark	---

8.8 CTP – Internal static capacity

8.8.1 Internal static capacity test set-up

The set-up for this test system is shown in Figure 41.



Key

1	CXPI network
Components	
D	Diode (1N4148)
C_{COMMON}	common capacitance
C_{REF}	reference capacitance
R_{COMMON}	common resistor
R_{REF}	reference resistor
S1	switch 1
S2	switch 2
S3A	switch 3A
S3B	switch 3B

Figure 41 — Test system – Internal static capacity test set-up

8.8.2 1.CTC_8.1 Internal static capacity

The set-up for the switch of this test system of internal static capacity is described in Table 92.

Table 92 — Test system – Internal static capacity test

Switch	Setting
S3 A/B	In case that the IUT is connected by a wire harness: — the IUT is disconnected from the wire harness, and S3A and S3B are turned on (short out) and measured; — this is to eliminate the static capacity of the wire harness.

Table 93 specifies the CTC that verifies the 1.CTC_8.1 Internal static capacity.

Table 93 — 1.CTC_8.1 Internal static capacity

Item	Content
CTC # – Title	1.CTC_8.1 Internal static capacity
Purpose	This CTC verifies that the internal static capacity of the IUT complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 1.18 PHY – PMD device interface electrical parameter $C_{SLAVE.}$
Prerequisite	The test system set-up shall be in accordance with Figure 41.

Set-up	— The IUT shall be configured as a slave node.
	— The bit rate shall be set to the default value (see 6.6.2).
	— The SUT shall be initialised to default (see 6.7).
	— V_{IUT}: [V_{SUP}/V_{BAT}]: 14 V.
	— R_{COMMON}: 1 kΩ (±0,1 %).
	— C_{COMMON}: 750 pF (1,5 nF + 1,5 nF in series) (±1 %).
	— R_{REF}:
	  — It shall be the same value with the pull-up resistance (±5 %) in the IUT;
	  — If the measurement is impossible, it uses 30 kΩ (±0,1 %).
	— $C_{REF.}$ 250 pF (100 pF || 150 pF parallel) (±1 %).
	— S1, S2: see Table 94.

Step	1. The pulse generator shall be driven with a 50 % duty cycle square wave at 10 kHz. The rising time shall be less or equal than 20 ns. Slope time shall be measured at 10 % and 90 % of slope voltage. 2. S3B on (short out). 3. The measurement shall observe both the ends of the R_{COMMON} and shall measure the rising time t_{REF} under the environment of static capacity (250 pF + 750 pF). 4. S3A on (short out). 5. The measurement shall observe both ends of the R_{COMMON} and shall measure the rising time t_{INT} under the environment of internal static capacity of the IUT + 750 pF.
Iteration	All steps shall be executed for each test case specified in Table 94.
Expected response	After step 5: The measurement shall observe both ends of the R_{COMMON} and shall measure: C_{SLAVE} less or equal than 250 pF:($t_{INT} \leq t_{REF}$). $t_{REF} \leq t_{INT.}$ The IUT shall not interfere by the output of fraud waveform.
Remark	---

Table 94 — TC – 1.CTC_8.1 – Internal static capacity test

CTC-EPL-TC	Condition	S1	S2
1.CTC_8.1-1	The IUT is in the normal state by supplying the normal voltage	V_{PS}	GND
1.CTC_8.1-2	Loss of the GND (the GND of the IUT shorts out to power)	V_{PS}	V_{PS}
1.CTC_8.1-3	Loss of the V_{PS} (power of the IUT V_{IUT} shorts out to the GND)	GND	GND

8.9 CTP – Internal resistance measurement during operation

8.9.1 Internal resistor measurement test set-up

The measurement of the internal resistance is based on the measurement of the external resistance using Formula (1) to Formula (6).

$$V_{RINT\_meas1} = V_{IUT} - V_{diode} - V_{meas1} = (I_{meas1} - I_{leak1}) \times R_{INT} \quad (1)$$

where

V_{RINT_meas1} is the voltage at R_{INT} with R_{meas1};

V_{IUD} is the voltage at the IUD;

V_{diode} is the voltage at the diode;

V_{meas1} is the voltage at meas1;

I_{meas1} is the current at meas1;

I_{leak1} is the leak current at leak1;

R_{INT} is the internal resistor.

$$V_{RINT\_meas2} = V_{IUT} - V_{diode} - V_{meas2} = (I_{meas2} - I_{leak2}) \times R_{INT} \quad (2)$$

where

V_{RINT_meas2} is the voltage at R_{INT} with R_{meas2};

V_{diode} is the voltage at the diode;

V_{meas2} is the voltage at meas2;

I_{meas2} is the current at meas2;

I_{leak2} is the leak current at leak2;

R_{INT} is the internal resistor.

Formula (1) - Formula (2):

$$(V_{IUT} - V_{diode} - V_{meas1}) - (V_{IUT} - V_{diode} - V_{meas2}) = (I_{meas1} - I_{leak1}) \times R_{INT} - (I_{meas2} - I_{leak2}) \times R_{INT} \quad (3)$$

$$V_{meas2} - V_{meas1} = (I_{meas1} - I_{meas2}) \times R_{INT} - (I_{leak1} - I_{leak2}) \times R_{INT} \quad (4)$$

With the following assumption:

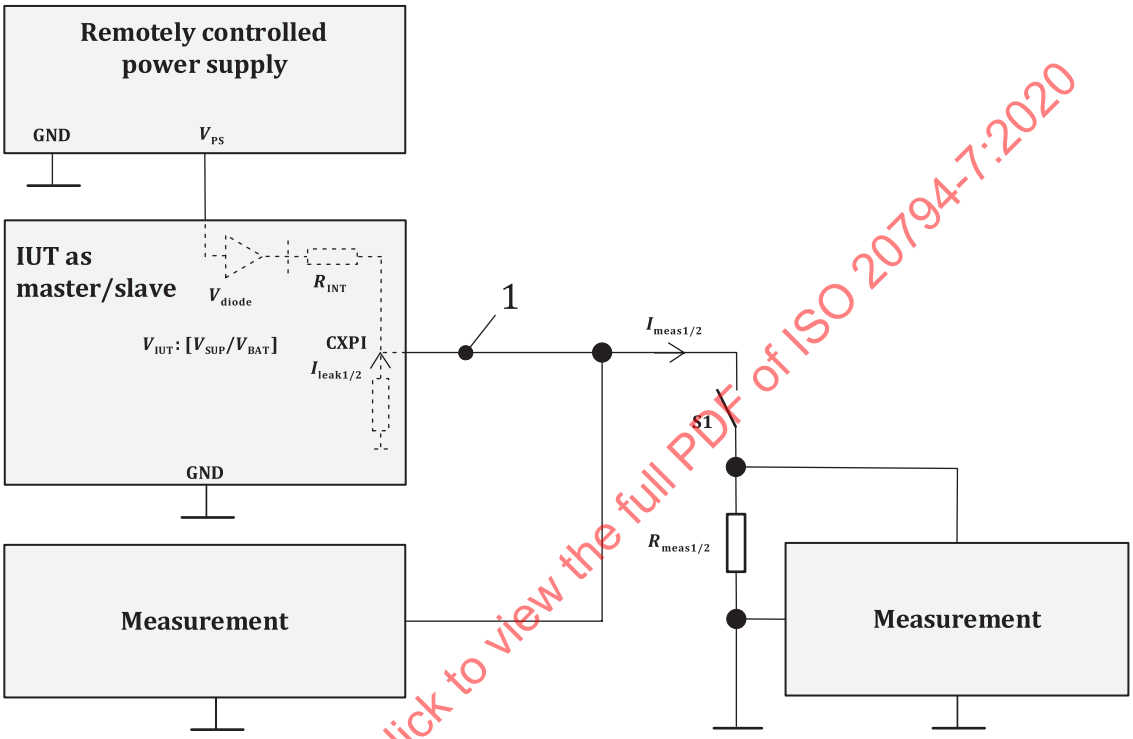
$$I_{leak} \sim \text{constant} \rightarrow I_{leak1} = I_{leak2} \quad (5)$$

where I_{leak} is the leak current.

The internal resistor can be calculated as follows:

$$R_{INT} = \frac{V_{meas2} - V_{meas1}}{I_{meas1} - I_{meas2}} \quad (6)$$

This set-up of the test system is shown in Figure 42.



Key

1	CXPI network
Component	
$R_{meas1/2}$	resistor for measurement (half value)
S1	switch S1

Figure 42 — Test system – Measuring internal resistor test set-up

8.9.2 1.CTC_9.1– Internal resistor measurement 1

Table 95 specifies the CTC that verifies the 1.CTC_9.1– Internal resistor measurement 1.

Table 95 — 1.CTC_9.1– Internal resistor measurement 1

Item	Content
CTC # – Title	1.CTC_9.1– Internal resistor measurement 1
Purpose	This CTC verifies that the internal resistor complies with the CXPI specification.
Reference	ISO 20794-4:2020 — REQ 1.17 PHY – PMD entity requirements; — REQ 1.18 PHY – PMD device interface electrical parameter R_{SLAVE}.
Prerequisite	The test system set-up shall be in accordance with Figure 42.

Table 95 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}]: 14 V. — $R_{meas1:}$ 10 kΩ (±0,1 %). — $R_{meas2:}$ 20 kΩ (±0,1 %).
Step	1. The UT shall control the IUT to stop the transmission to the CXPI network.
Iteration	Not applicable
Expected response	After step 1: The measurement shall measure the resistance value of R_{INT}: 20 kΩ ≤ R_{INT} ≤ 60 kΩ [see Formula (6)]. The measurement shall measure the resistance before the timeout is detected if the dominant state timeout function of the IUT affects the measurement (if the IUT incorporates a CXPI network dominant state timeout detection, the IUT's pull–up resistor shall disable).
Remark	---

8.9.3 1.CTC_9.2– Internal resistor measurement 2

Table 96 specifies the CTC that verifies the 1.CTC_9.2– Internal resistor measurement 2.

Table 96 — 1.CTC_9.2– Internal resistor measurement 2

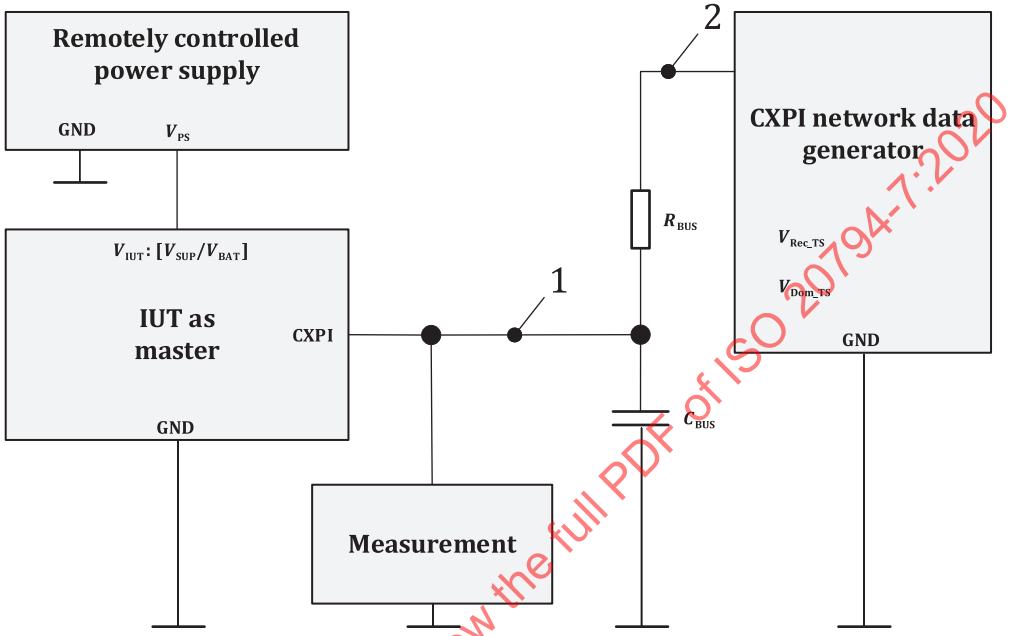
Item	Content
CTC # – Title	1.CTC_9.2– Internal resistor measurement 2
Purpose	This CTC verifies that the internal resistor complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 1.17 PHY – PMD entity requirements; — REQ 1.18 PHY – PMD device interface electrical parameter R_{MASTER}.
Prerequisite	The test system set-up shall be in accordance with Figure 42.
Set-up	— The IUT shall be configured as a master node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}]: 14 V. — R_{meas1}: 1 kΩ (±0,1 %). — R_{meas2}: 2 kΩ (±0,1 %).
Step	1. The UT shall control the IUT to stop the clock to the CXPI network.
Iteration	Not applicable
Expected response	After step 1: The measurement shall measure the resistance value of R_{INT}: 900 Ω ≤ R_{INT} ≤ 1 100 Ω [see Formula (6)]. The measurement shall measure the resistance before the timeout is detected if the dominant state timeout function of the IUT affects the measurement (if the IUT incorporates a CXPI network dominant state timeout detection, the IUT's pull–up resistor shall disable.).
Remark	---

9 Physical layer conformance test plan (PS –PMA non-separate type)

9.1 CTP – Operational conditions and calibration

9.1.1 1.CTC_10.1 – Clock transmission

The test system set-up for this test is shown in Figure 43.

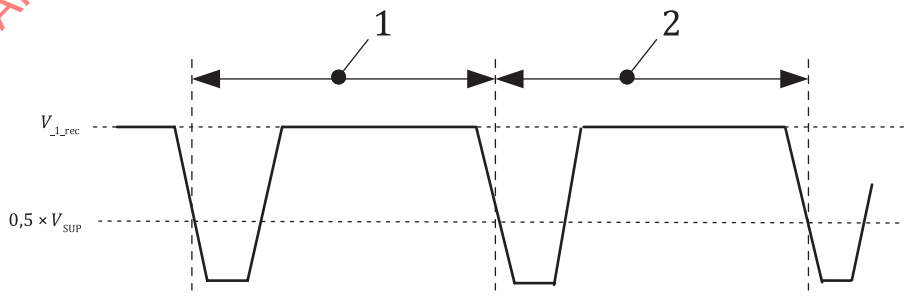


Key

1	CXPI network
2	$V_{\text{Pull-up}}$
Components	
C_{BUS}	total bus capacitance
R_{BUS}	total CXPI network resistance

Figure 43 — Test system – Clock transmission test set-up

The PWM waveform $\Delta t_{\text{bit\_dif}}$ of clock transmission for this test is shown in Figure 44.



Key

1 $t_{\text{bit\_ref}}$ (bit width of reference bit rate)

2 $t_{\text{bit\_ref}} \times (1 + \Delta t_{\text{bit}})$

Figure 44 — Test system – Clock transmission PWM waveform

Table 97 specifies the CTC that verifies the 1.CTC_10.1 – Clock transmission.

Table 97 — 1.CTC_10.1 – Clock transmission

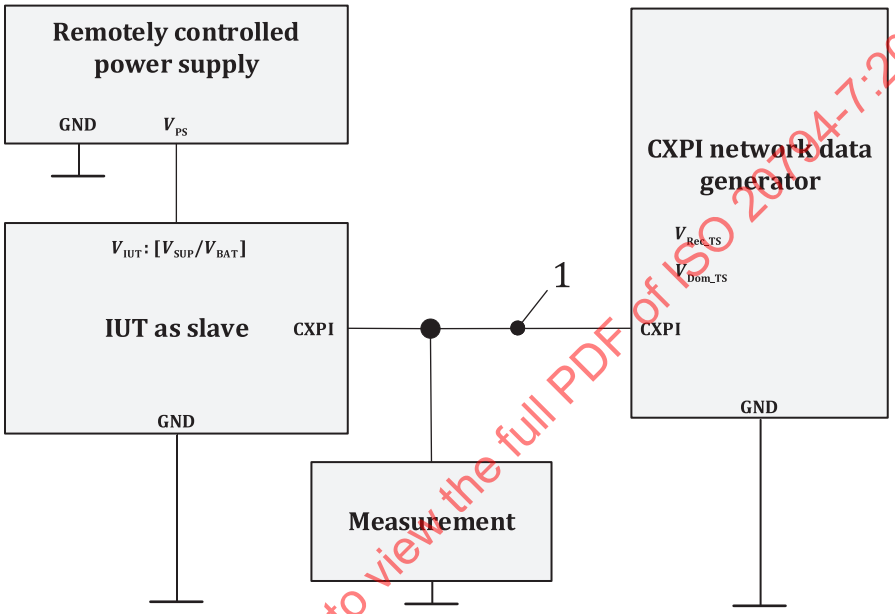
Item	Content
CTC # – Title	1.CTC_10.1 – Clock transmission
Purpose	This CTC verifies that the clock output function of the IUT complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 1.1 PHY – PS bit rate; — REQ 1.5 PHY – PS clock generation; — REQ 1.6 PHY – PS clock generation - Transmitter jitter Δt_{bit_cont}; _ REQ 1.14 PHY – PMA AC parameters $D_{tx\_1\_lo\_dom}$, $D_{tx\_1\_lo\_rec}$; — REQ 1.14 PHY – PMA AC parameters $t_{tx\_pwm\_slope\_clk}$.
Prerequisite	The test system set-up shall be in accordance with Figure 43.
Set-up	— The IUT shall be configured as a master node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to L_PwrMng1 (see 6.7). — V_{IUT} (V_{SUP} or V_{BAT}): see Table 98. — R_{BUS}: see Table 98. — C_{BUS}: see Table 98. — V_{Dom_TS}: see Table 98. — V_{Rec_TS} or $V_{Pull\text{-}up}$: see Table 98.
Step	1. The IUT shall be powered. 2. The UT shall control the IUT to transmit the PWM waveform for the clock transmission on the CXPI network. 3. The UT shall control the IUT to transmit the PWM waveform with the logical value 1 consecutively.
Iteration	All steps shall be executed for each test case specified in Table 98.
Expected response	After step 2: The IUT shall transmit the PWM waveform for the clock transmission on the CXPI network. The measurement shall observe and shall measure the clock: $D_{tx\_1\_lo\_dom} \geq 0{,}11$, $D_{tx\_1\_lo\_rec} \leq 0{,}45$, $t_{tx\_pwm\_slope\_clk} \leq 8$ µs. The voltage level of clock width shall be 0,5 V_{rec_master}. After step 3: The IUT shall transmit the PWM waveform with the logical value 1 consecutively. The measurement shall observe and shall measure the clock: Δt_{bit} (Δt_{bit_cont} + Δt_{bit_driver}) of the clock transmission: within ±1 % of reference bit rate.
Remark	---

Table 98 — TC – 1.CTC_10.1 – Clock transmission

CTC-EPL-TC	V_{IUT}: [V_{SUP}/V_{BAT}]	V_{Dom_TS}	V_{Rec_TS}/$V_{Pull\text{-}up}$	R_{BUS}	C_{BUS}
1.CTC_10.1-1	8 V	0 V	8 V	30 kΩ (±0,1 %)	4 nF (±1 %)
1.CTC_10.1-2	13 V	0 V	13 V		
1.CTC_10.1-3	18 V	0 V	18 V		

9.1.2 1.CTC_10.2 – Detection of clock existence

The test system set-up for this test is shown in Figure 45.



Key

1 CXPI network

Figure 45 — Test system – Detection of clock existence test set-up

Table 99 specifies the CTC that verifies the 1.CTC_10.2 – Detection of clock existence.

Table 99 — 1.CTC_10.2 – Detection of clock existence

Item	Content
CTC # – Title	1.CTC_10.2 – Detection of clock existence
Purpose	This CTC verifies that the detection function of the clock existence.
Reference	ISO 20794-4:2020, REQ 1.9 PHY – PS detection of clock existence.
Prerequisite	The test system set-up shall be in accordance with Figure 45.
Set-up	— The IUT shall be configured as a slave node (1.CTC_10.2-1 or 1.CTC_10.2-2). — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to L_PwrMng1 (see 6.7).
Step	1. The IUT shall be powered. 2. The CXPI network data generator shall start transmitting the clock in a waveform as specified in Table 100.
Iteration	Step 1 and step 2 shall be executed for each test case specified in Table 100.

Table 99 *(continued)*

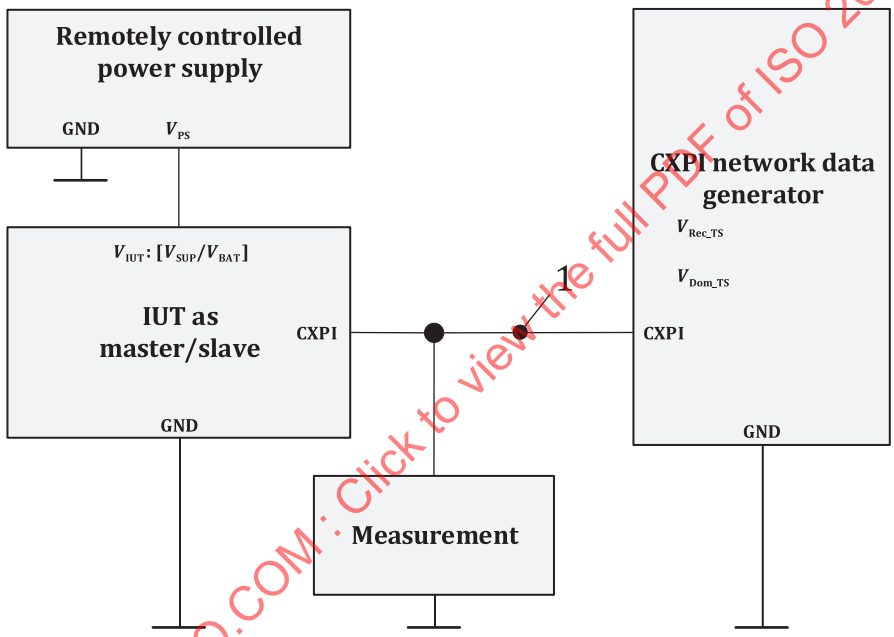
Item	Content
Expected response	After step 2: The IUT shall detect the clock existence.
Remark	---

Table 100 — TC – 1.CTC_10.2 – Detection of clock existence

CTC-EPL-TC	Requirements for the clock waveform	Inclination ratio
1.CTC_10.2-1	$D_{tx\_1\_lo\_dom}$ = 0,11	<5 V/µs
1.CTC_10.2-2	$D_{tx\_1\_lo\_rec}$ = 0,45	

9.1.3 1.CTC_10.3 – Arbitration function (stop transmission by arbitration)

The test system set-up for this test is shown in Figure 46.



Key

1 CXPI network

Figure 46 — Test system – Arbitration function (stop transmission by arbitration) test set-up

Table 101 specifies the CTC that verifies the 1.CTC_10.3 – Arbitration function (stop transmission by arbitration).

Table 101 — 1.CTC_10.3 – Arbitration function (stop transmission by arbitration)

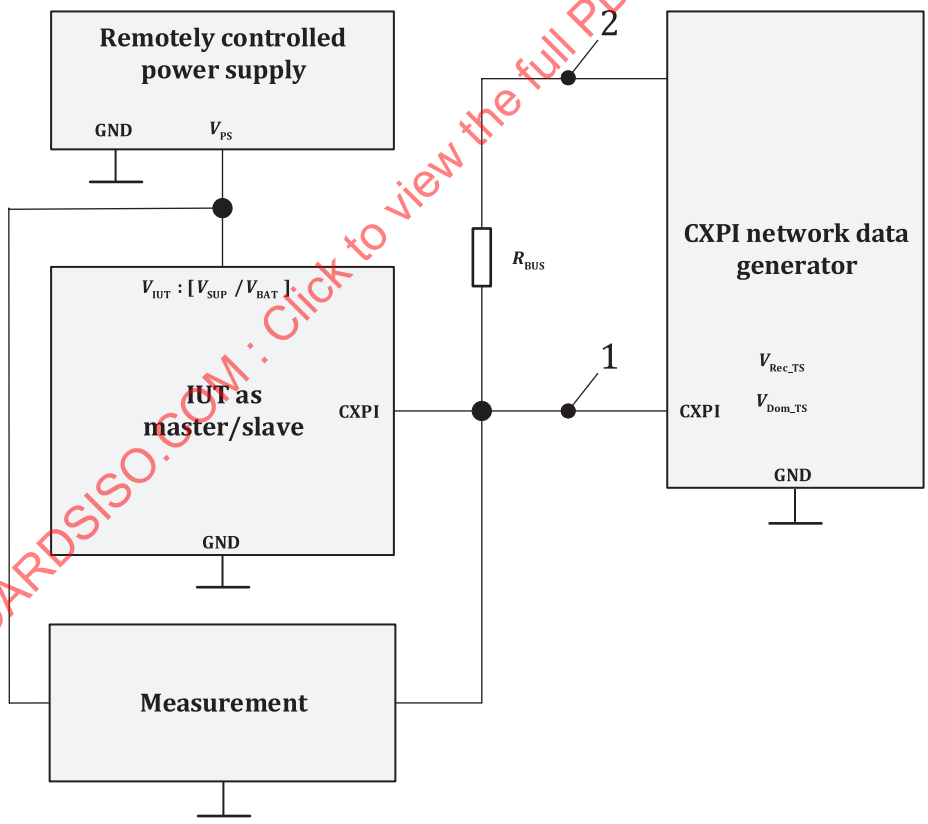
Item	Content
CTC # – Title	1.CTC_10.3 – Arbitration function (stop transmission by arbitration)
Purpose	This CTC verifies that the arbitration of the bit collisions complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 1.10 PHY – PS bit-wise collision resolution.
Prerequisite	The test system set-up shall be in accordance with Figure 46.

Table 101 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a master node or a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to default (see 6.7).
Step	1. The UT shall control the IUT to transmit a logical value of 1or a logical value of 0. 2. The CXPI network data generator shall collide any bit in logical value '0' of RX_{PWM} with any bit in logical value '1' of RX_{PWM} excluding the parity bit.
Iteration	Not applicable
Expected response	After step 2: The IUT shall stop the transmission of logical value '0' after any bit in logical value '0' of RX_{PWM}. The CXPI network data generator shall continue the transmission after a dominant bit collision.
Remark	---

9.1.4 1.CTC_10.4 – Operating voltage range

The test system set-up for this test is shown in Figure 47.



Key

1	CXPI network
2	$V_{Pull\text{-}up}$
Component	
R_{BUS}	total CXPI network resistance

Figure 47 — Test system – Operating voltage range test set-up

Table 102 specifies the CTC that verifies the 1.CTC_10.4 – Operating voltage range.

Table 102 — 1.CTC_10.4 – Operating voltage range

Item	Content
CTC # – Title	1.CTC_10.4 – Operating voltage range
Purpose	This CTC verifies that the IUT operates correctly in the valid supply voltage ranges.
Reference	ISO 20794-4:2020: — REQ 1.8 PHY – PS node clock synchronisation and bit synchronization; — REQ 1.13 PHY – PMA electrical parameters V_{BAT}; — REQ 1.13 PHY – PMA electrical parameters V_{SUP}.
Prerequisite	The test system set-up shall be in accordance with Figure 47.
Set-up	— The IUT shall be configured as a master node (1.CTC_10.4-1 or 1.CTC_10.4-2) or a slave node (1.CTC_10.4-3 or 1.CTC_10.4-4). — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to L_PwrMng1 (see 6.7). — V_{IUT}: [V_{SUP}/V_{BAT}]: see Table 103. — R_{BUS}: see Table 103. — V_{Dom_TS}: 0 V. — V_{Rec_TS}/$V_{Pull\text{-}up}$: see Table 103.
Step	1. The remotely controlled power supply shall be set on the V_{BAT}/V_{SUP} as specified in Table 103. 2. The UT shall control the IUT to transmit and receive the PWM waveform.
Iteration	Step 1 and step 2 shall be executed for each test case specified in Table 103.
Expected response	During step 2: The IUT shall transmit and receive the PWM waveform continuously under all conditions. The CXPI network data generator shall transmit and receive the PWM waveform continuously under all conditions.
Remark	---

Table 103 — TC – 1.CTC_10.4 – Operating voltage range

CTC-EPL-TC	V_{IUT} range: [V_{SUP} range/V_{BAT} range]	V_{Rec_TS}/$V_{Pull\text{-}up}$	Signal ramp	R_{BUS}
1.CTC_10.4-1	[7,0 V to 18 V]/[8,0 V to 18 V]	[8,0 V to 18 V]	0,1 V/s	30 kΩ (±0,1 %)
1.CTC_10.4-2	[18 V to 7,0 V]/[18 V to 8,0 V]	[18 V to 8,0 V]	0,1 V/s	30 kΩ (±0,1 %)
1.CTC_10.4-3	[7,0 V to 18 V]/[8,0 V to 18 V]	[8,0 V to 18 V]	0,1 V/s	1 kΩ (±0,1 %)
1.CTC_10.4-4	[18 V to 7,0 V]/[18 V to 8,0 V]	[18 V to 8,0 V]	0,1 V/s	1 kΩ (±0,1 %)

9.2 CTP – Wake-up pulse

9.2.1 General

9.2 describes the behaviour of the IUT when it receives the wake-up pulse. All CTCs specified in 9.2 are applicable only to the IUTs, which support ISO 20794-2.

9.2.2 1.CTC_11.1 – Wake-up pulse reception, IUT as master node

Table 104 specifies the CTC that verifies the 1.CTC_11.1 – Wake-up pulse reception, IUT as master node.

Table 104 — 1.CTC_11.1 – Wake-up pulse reception, IUT as master node

Item	Content
CTC # – Title	1.CTC_11.1 – Wake-up pulse reception, IUT as master node
Purpose	This CTC verifies that the behaviour of the IUT when receiving the wake-up pulse complies with the CXPI specification.
Reference	ISO 20794-4:2020, REQ 1.16 PHY – PMA wake-up pulse and dominant pulse filter time $t_{rx\_wakeup\_clk}$.
Prerequisite	The test system set-up shall be in accordance with Figure 2. This test is only applicable to a master node.
Set-up	— The IUT shall be configured as a master node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to L_PwrMng2 (see 6.7).
Step	1. The LT shall transmit the wake-up pulse as specified in Table 105.
Iteration	Step 1 shall be executed for each test case specified in Table 105.
Expected response	See Table 105.
Remark	---

Table 105 defines the test cases: wake-up pulse reception, IUT as master.

Table 105 — TC – 1.CTC_11.1 – Wake-up pulse reception, IUT as master

CTC-EPL-TC	Wake-up pulse parameter	Value	Judgement criteria	
1.CTC_11.1-1	t_{tx_wakeup}	400 µs	After step 1:	The IUT shall notify the `ev_wakeup_pulse_detect`.
	$t_{tx\_wakeup\_space}$	5 ms		
1.CTC_11.1-2	t_{tx_wakeup}	2 500 µs		
	$t_{tx\_wakeup\_space}$	5 ms		
1.CTC_11.1-3	t_{tx_wakeup}	400 µs		
	$t_{tx\_wakeup\_space}$	10 ms		
1.CTC_11.1-4	t_{tx_wakeup}	2 500 µs		
	$t_{tx\_wakeup\_space}$	10 ms		
1.CTC_11.1-5	t_{tx_wakeup}	29 µs	After step 1:	The IUT shall not wake-up.

9.2.3 1.CTC_11.2 – Wake-up by clock detection

Table 106 specifies the CTC that verifies the 1.CTC_11.2 – Wake-up by clock detection.

Table 106 — 1.CTC_11.2 – Wake-up by clock detection

Item	Content
CTC # – Title	1.CTC_11.2 – Wake-up by clock detection
Purpose	This CTC verifies that the behaviour of the IUT when receiving the wake-up pulse (i.e. clock) complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 1.16 PHY – PMA wake-up pulse and dominant pulse filter time t_{rx_wakeup}; — REQ 1.16 PHY – PMA wake-up pulse and dominant pulse filter time $t_{rx\_wakeup\_space}$.
Prerequisite	The test system set-up shall be in accordance with Figure 2. This test is only applicable to a slave node.

Table 106 *(continued)*

Item	Content
Set-up	— The IUT shall be configured as a slave node. — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to L_PwrMng2 (see 6.7).
Step	1. The LT shall transmit the clock waveform specified in the Conditions column of Table 107.
Iteration	Step 1 shall be executed for each test case specified in Table 107.
Expected response	See Table 107.
Remark	---

Table 107 — TC – 1.CTC_11.2 – Wake-up by clock detection

CTC-EPL-TC	Conditions		Expected response
1.CTC_11.2-1	$D_{tx\_1\_lo\_dom}$ = 0,11	Inclination rate of waveform < 5 V/µs	After step 1: The IUT shall notify the wake-up reception.
1.CTC_11.2-2	$D_{tx\_1\_lo\_rec}$ = 0,45		
1.CTC_11.2-3	The LT shall transmit the dominant level with 0,4 µs duration in 1 t_{bit} interval.		Afterstep 1: The IUT shall not wake-up.
1.CTC_11.2-4	The LT shall transmit the dominant level with 0,25 t_{bit} duration in 61 ms interval.		After step 1: The IUT shall not wake-up.

9.2.4 1.CTC_11.3 – Wake-up pulse transmission

Table 108 specifies the CTC that verifies the 1.CTC_11.3 – Wake-up pulse transmission.

Table 108 — 1.CTC_11.3 – Wake-up pulse transmission

Item	Content
CTC # – Title	1.CTC_11.3 – Wake-up pulse transmission
Purpose	This CTC verifies that the function of the transmission of the wake-up pulse by a slave node complies with the CXPI specification.
Reference	ISO 20794-4:2020: — REQ 1.7 PHY – PS clock generation – Clock stop; — REQ 1.12 PHY – PS node transmission of wake-up pulse t_{tx_wakeup}; — REQ 1.12 PHY – PS node transmission of wake-up pulse $t_{tx\_wakeup\_space}$.
Prerequisite	The test system set-up shall be in accordance with Figure 2.
Set-up	— The IUT shall be configured as a slave node (1.CTC_11.3-1 or 1.CTC_11.3-2). — The bit rate shall be set to the default value (see 6.6.2). — The SUT shall be initialised to L_PwrMng2 (see 6.7).
Step	1. The UT shall control the IUT to transmit the wake-up pulse as specified in Table 109.
Iteration	Step 1 shall be executed for each test case specified in Table 109.
Expected response	See Table 109.
Remark	---

Table 109 — TC – 1.CTC_11.3 – Wake-up pulse transmission

CTC-EPL-TC	Definition	Judgement criteria	
1.CTC_11.3-1	The LT receives the first dominant pulse which IUT shall transmit, and then the LT starts clock supply after 4 ms have elapsed.	After step 1	The IUT shall transmit the wake-up pulse which meets 400 µs ≤ t_{tx_wakeup} ≤ 2 500 µs. The LT shall receive the wake-up pulse which meets 400 µs ≤ t_{tx_wakeup} ≤ 2 500 µs. The start point of the measurement shall be the fall edge of the waveform and the end point of the measurement shall be the rise edge of the waveform. The IUT shall not transmit the second dominant pulse. The LT shall not receive the second dominant pulse.
1.CTC_11.3-2	The LT shall receive second dominant pulse which the IUT shall transmit and then the shall start clock supply within 59 ms.	After step 1	The IUT shall transmit the wake-up pulse, which meets 400 µs ≤ t_{tx_wakeup} ≤ 2 500 µs and 5 ms ≤ $t_{tx\_wakeup\_space}$ ≤ 10 ms. The LT shall transmit the wake-up pulse, which meets 400 µs ≤ t_{tx_wakeup} ≤ 2 500 µs and 5 ms ≤ $t_{tx\_wakeup\_space}$ ≤ 10 ms. The start point of the measurement shall be the fall edge of the waveform and the end point of the measurement shall be the rise edge of the waveform.

9.3 CTP – Voltage and duty cycle thresholds

9.3.1 General

All tests described in 9.3 verify the threshold voltages and threshold duty cycle of the IUT are implemented correctly within the specified operating supply voltage range.

9.3.2 1.CTC_12.1 – Voltage threshold test 1

This set-up of the test system is shown in Figure 48.