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Electrostatic discharge (ESD) sensitivity testing machine model (MM)

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Test Method A115-A

Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

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ELECTRONIC INDUSTRIES ASSOCIATION

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY
TESTING MACHINE MODEL (MM)

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Draft PAS		**Report on voting**	
47/1453/PAS		47/1486/RVD	

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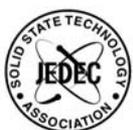
TEST METHOD A115A

**ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING
MACHINE MODEL (MM)**

(From JEDEC Council Ballot JCB-97-10, formulated under the cognizance of JC-14.1 Committee on
Reliability Test Methods for Packaged Devices.)

1 Purpose

This method establishes a standard procedure for testing and classifying microcircuits according to their
susceptibility to damage or degradation by exposure to a defined Machine Model (MM) electrostatic
discharge (ESD). The objective is to provide reliable, repeatable MM ESD test results so that accurate
classifications can be performed.

2 Apparatus

This test method requires the following equipment.

2.1 An ESD Pulse Simulator and a Device Under Test (DUT) socket equivalent to the circuit of figure 1.
The simulator must be capable of supplying pulses with the characteristics required by figure 2 and
figure 3.

2.2 Oscilloscope

The oscilloscope and amplifier combination shall have a 350 MHz minimum single-shot bandwidth and a
visual writing speed of 4 cm/ns minimum.

2.3 Current probe

The current probe shall have a minimum pulse-current bandwidth of 350 MHz. A current probe
(transformer and cable with a nominal length of 1 meter) with a 1 GHz bandwidth and a current rating of
12 amperes maximum pulse-current is recommended.

2.4 Evaluation Loads

An 18 AWG tinned copper wire is recommended for the short waveform verification test. The lead
length should be as short as practicable to span the distance between the two farthest pins in the socket
while passing through the current probe. The ends of the 18 AWG wire may be ground to a point where
clearance is needed to make contact on fine pitch socket pins.

A 500 ohm +/-1%, 1000 volt, low inductance resistor shall be used for initial system checkout and
periodic system recalibration.

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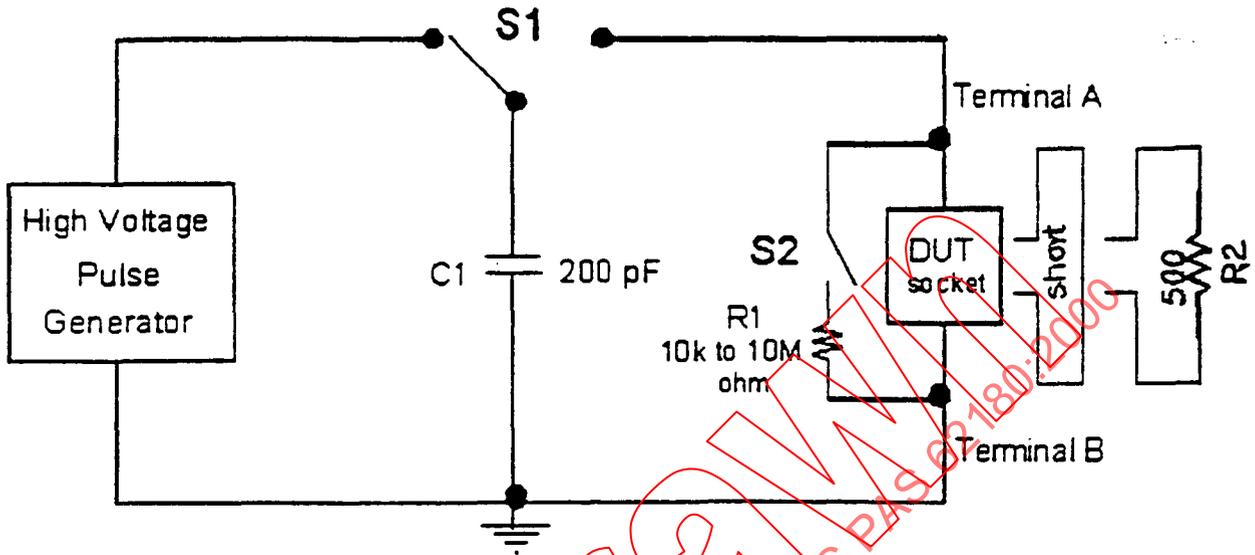(Revision of Test Method A115)

2 Apparatus (cont'd)

Figure 1 — Typical equivalent MM ESD circuit

NOTES

1 The performance of any simulator is influenced by its parasitic capacitance and inductance.

2 Precautions must be taken in tester design to avoid recharge transients and multiple pulses.

3 R2, used for initial equipment qualification and requalification as specified in 3.1, shall be a low inductance, 1000 volt, 500 ohm resistor with +/-1% tolerance.

4 Stacking of DUT socket adaptors (piggybacking) is allowed only if the waveforms can be verified to meet the specifications in table 1.

5 Reversal of terminal A and B to achieve dual polarity is not permitted.

6 S2 should be closed 10 to 100 milliseconds after the pulse delivery period to ensure the DUT socket is not left in a charged state.
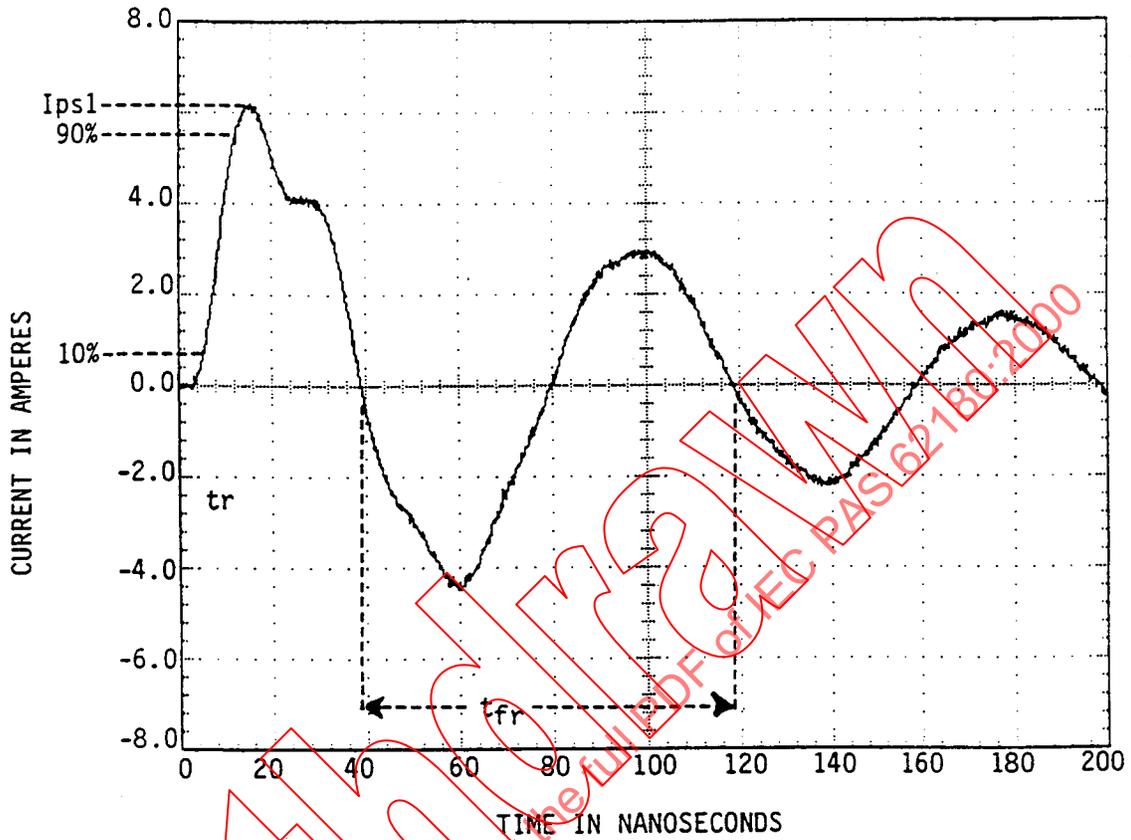
7 C1, 200 pF +/- 10%.

2 Apparatus (cont'd)

Figure 2 — Current Waveform through a shorting wire, 400 volt discharge
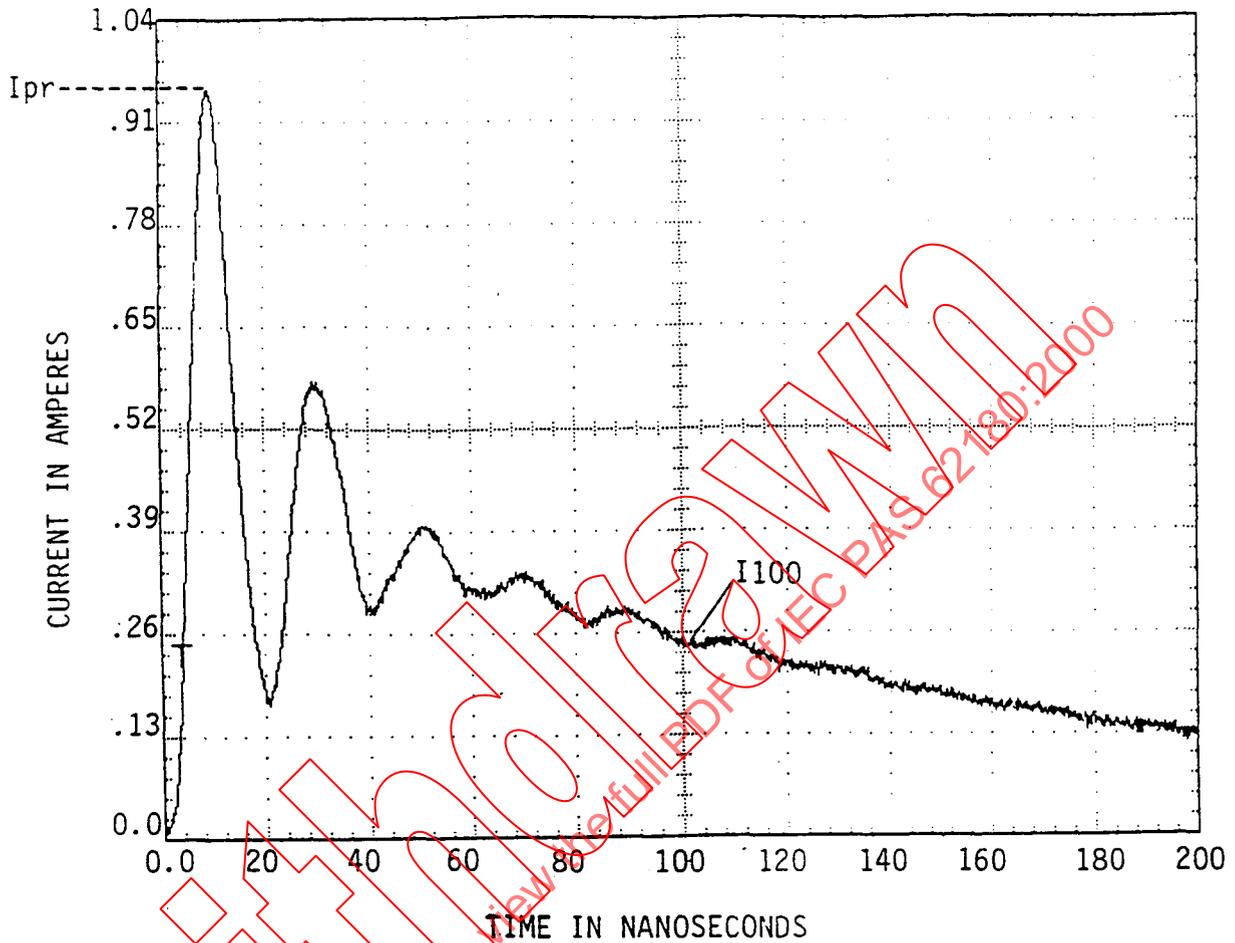
2 Apparatus (cont'd)

Figure 3 — Current waveform through a 500 ohm resistor, 400 volt discharge

3 Qualification, calibration, and waveform verification

3.1 Equipment qualification

Equipment calibration must be performed during initial acceptance testing. Recalibration is required whenever equipment repairs are made that may affect the waveform and a minimum of every 12 months. The tester must meet the requirements of table 1 and figure 2 at all voltage levels using the shorting wire and at the 400 volt level with the 500 ohm resistor (see figure 3). The waveform measurements during calibration shall be made using the worst-case pin on the highest pin count board with a positive mechanical clamp socket. (Machine repeatability should be verified during initial equipment acceptance by performing a minimum of 5 consecutive positive and a minimum of 5 consecutive negative waveforms at a voltage level in table 1.) The high-voltage relays and associated high-voltage circuitry shall be tested by the user of computer-controlled systems per the equipment manufacturer's instructions (system diagnostics). This test will check for any open or short relays.

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3 Qualification, calibration, and waveform verification (cont'd)

Table 1 — Waveform specification

Voltage Level (v)	Positive Ipeak for Short, Ipsl (A)	Positive Ipeak for 500 Ohm* Ipr (A)	Current at 100 ns for 500 Ohm* I100 (A)	Maximum Ringing Current, I_R (A)	Resonance Frequency for Short, FR (l/tfr) (Mhz)
100	1.5- 2.0	N/A	N/A	Ipsl x 30%	11-16
200	2.8- 3.8	N/A	N/A	Ipsl x 30%	11-16
400	5.8- 8.0	I100 x 4.5 maximum	0.29+/-20%	Ipsl x 30%	11-16

* The 500 ohm load is used only during Equipment Qualification as specified in 3.1.

3.1.1 Safety Training

During initial equipment set-up, the safety engineer or applicable safety representative, shall inspect the equipment in its operating location to ensure that the equipment is not operated in a combustible (hazardous) environment.

Additionally, all personnel shall receive system operational training and electrical safety training prior to using the equipment.

3.2 Worst-case pin

The worst-case pin combination for each socket and DUT board shall be identified and documented. It is recommended that the manufacturers supply the worst-case pin data with each DUT board. The pin combination with the waveform closest to the limits (see table 1) shall be designated for waveform verification.

The worst-case pin combination shall be identified by the following procedure.

3.2.1 For each test socket, identify the socket pin with the shortest wiring path from the pulse generating circuit to the test socket. Connect this pin to Terminal B (where it will remain the referenced pin throughout the worst case pin search) and connect one of the remaining pins to Terminal A. Attach a shorting wire between these pins with the current probe around the shorting wire, as close to Terminal B as practicable.

3 Qualification, calibration, and waveform verification (cont'd)

3.2.2 Apply a positive 400 volt pulse and a negative 400 volt pulse and verify that the waveform meets the requirements defined in table 1 for both positive and negative pulses.

3.2.3 Repeat steps 3.2.1 and 3.2.2 until all socket pins have been evaluated.

3.2.4 Determine the worst-case pin pair (within the limits and closest to the minimum or maximum parameter values as specified in table 1) to be used for future waveform verification.

3.2.5 For initial board check-out, connect a 500 ohm resistor between the worst-case pins previously identified with the shorting wire in step 3.2.4. Apply a positive and negative 400 volt pulse and verify that the waveform meets the requirements defined in table 1.

> NOTE — In case the test socket/test board has already been characterized for worst-case pin on HBM, then that pin combination is acceptable for use with MM waveform verification.

As an alternative to the worst-case pin search, the reference pin pair may be identified for each test socket of each test fixture. The reference pin combination shall be identified by determining the socket pin with the shortest wiring path from the pulse generating circuit to the test socket. Connect this pin to Terminal B and then connect the socket pin with the longest wiring path from the pulse generating circuit to the test socket to Terminal A (normally provided by the manufacturer). Attach a shorting wire between these pins with the current probe around the shorting wire. Follow the procedure in step 3.2.2. For the initial board check-out connect a 500 ohm resistor between the reference pins. Apply a positive and negative 400 volt pulse and verify that the waveform meets the parameters in table 1.

3.3 Waveform verification

The waveform verification shall be performed at the beginning of each shift a tester is operated and when a socket/DUT board is changed. If at any time the waveforms do not meet the requirements defined in figure 1 and table 1 at the 400 volt level, the testing shall be halted until the waveform is in compliance. Additionally, the system diagnostics test as defined in 3.1 for automated systems shall be performed prior to the beginning of each shift testing is done. The period between waveform checks may be extended providing test data supports the increased interval. In case the waveform no longer meets the limits in table 1, all ESD testing performed after the previous satisfactory waveform check will be considered invalid.

3.3.1 With the required DUT socket installed and with no part in the socket, attach a shorting wire in the DUT socket such that the worst-case pins are connected between Terminal A and Terminal B as shown in figure 2. Place the current probe around the shorting wire.

3.3.2 Initiate a positive pulse at the 400 volt level per table 1 and figure 2. Verify that all parameters meet the limits specified in table 1 and figure 1.

3.3.3 Initiate a negative pulse at the 400 volt level per table 1. Verify that all parameters meet the limits specified in table 1 and figure 1.

4 Classification procedure

The devices used for classification testing must have completed all normal manufacturing operations.

4.1 Prior to ESD testing, dc parametric and functional testing at room temperature and, if applicable, high temperature shall be performed on all devices submitted for ESD testing. The test devices shall meet device data sheet requirements for these parameters.

4.2 A sample of 3 devices for each voltage level shall be characterized for the device ESD failure threshold using the voltage steps shown in table 1. Finer voltage steps may optionally be used to obtain a more accurate measure of the failure threshold. ESD Testing should begin at the lowest step in table 1. The ESD test shall be performed at room temperature.

4.3 Each sample of 3 devices shall be stressed at one voltage level using 1 positive and 1 negative pulses with a minimum of 0.5 second between pulses per pin for all pin combinations specified in table 2. It is permitted to use a separate sample of 3 devices for each pin combination specified in table 2. It is permitted to use the same sample (3) at the next higher voltage stress level if all parts pass the failure criteria specified in Section 5. after ESD exposure to a specified voltage level.

4.4 Pin combinations

The pin combinations to be used are given in table 2. The actual number of pin combinations depends on the number of power pin groups. Like named power pins (VCC1, VCC2, VSS1, VSS2, GND, etc.) that are directly connected by metal (inside the package) may be tied together and treated as one pin for Terminal B connection. Otherwise, each power pin must be treated as a separate power pin. Programming pins that do not draw current should be considered as I/O pins (example: Vpp pins on memory devices). Active discrete devices (FETs, transistors, etc.) shall be tested using all possible pin-pair combinations (one pin connected to Terminal A, another pin connected to Terminal B) regardless of pin name or function. All pins configured as "no connect" pins shall be verified as "no-connect" and left open (floating) at all times. Pins labeled "no-connect", that in fact are connected, shall be tested as non-supply pins.

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4 Classification procedure (cont'd)

4.4 Pin combinations (cont'd)

Table 2 — Pin Combinations for Integrated Circuits

Pin Combination	Connect Individually to Terminal A	Connect to Terminal B (Ground)	Floating Pins (unconnected)
1	All pins one at a time, except the pin(s) connected to Terminal B	First power pin(s)	All pins except 1/PUT* and first power pin(s)
2	All pins one at a time, except the pin(s) connected to Terminal B	Second power pin(s)	All pins except PUT and second power pin(s)
3	All pins one at a time, except the pin(s) connected to Terminal B	Nth power pin(s)	All pins except PUT and Nth power pin(s)
4	Each Non-supply pin, one at a time	All other Non-supply pins collectively except PUT	All power pins

* 1/PUT - Pin under test.

4.5 If a different sample group is ESD tested at each stress level, it is permitted to perform the dc parametric and functional ATE testing after all sample groups have been ESD tested.

5 Failure criteria

A part will be defined as a failure if, after exposure to ESD pulses, it no longer meets the device data sheet requirements using parametric and functional testing. If testing is required at multiple temperatures, testing shall be performed at the lowest temperature first.